Digital Equipment Corporation
Maynard, Massachusetts

digital

decsystem10

Maintenance Manual

RH10 MASSBUS CONTROLLER MAINTENANCE MANUAL

EK-RH10-MM-002

decsystem10

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CHAPTER 1
SYSTEM AND PHYSICAL DESCRIPTION

1.1 GENERAL

This manual describes the RH10 Device Controller, manufactured by Digital Equipment Corporation. Figure 1-1 shows a typical system configuration incorporating the PDP-10 Central Processor, the DF10 Data Channel, the RH10 Device Controller, and an RS04 drive. The RH10 Device Controller can control up to eight such drives.

1.1.1 Scope of Manual

The purpose of this manual is to provide Digital Field Service and customer maintenance personnel with sufficient installation, operation, and servicing information to install and maintain the RH10.

1.1.2 Related Documentation

Table 1-1 lists related documentation that supplements the information contained in this manual. It is assumed that the reader is acquainted with the material contained in these manuals.

1.2 RH10 CONTROLLER SPECIFICATIONS

The following paragraphs list the RH10 physical, environmental, and electrical specifications. The RH10 consists of four logic racks, an indicator panel, a maintenance panel, and a quick-latch assembly (for connecting to the DF10 bus) mounted in a 19-inch cabinet (Figure 1-2). The logic racks and the maintenance panel are located behind the front door of the cabinet.

1.2.1 Physical

Dimension and Weight

Width	22 in. (0.56 m)
Height	72 in. (1.83 m)
Depth	30 in. (0.76 m)
Weight	507 lbs (230 kg)

1.2.2 Environmental

Operating Temperature	60° to 90° F 15° to 35° C
Storage Temperature	40° to 110° F 5° to 45° C
Humidity	20% to 80%
Air Volume (Inlet)	800 cubic ft/min 380 I/S

1.2.3 Electrical

Power requirements at Line Cord

115 Vac ± 10%, 60 Hz ± 2% single-phase (30 A service recommended)

230 Vac ± 10%, 50 Hz ± 2% single-phase (15 A service recommended)

Power/heat dissipation	570 W 1900 Btu/hr
Line Current @ 115 Vac	5 A (13 A surge)

Unit Cable Lengths

PDP-10 Channel Bus	100 ft (30 m)
PDP-10 I/O Bus	150 ft (45 m)
Massbus	120 ft (36 m)

1.3 BUS INTERFACING

The RH10 Device Controller provides the interface between the PDP-10 Central Processor and the Massbus peripheral devices. It will control the Massbus device via the PDP-10 I/O Bus and will control and synchronize data transfers to memory via the DF10 Channel Bus.

Table 1-1
Related Documentation

Title	Document Number
DF10 Data Channel Maintenance Manual	DEC-10-HDFD-D
DF10-C Data Channel Maintenance Manual	A-MN-DF10-C-MAN1
DECsystem-10 Interface Manual	DEC-10-HIFC-D
DECsystem-10 Site Preparation Guide	EK-DEC10-SP-003
Assembly Language Handbook	DEC-10-NRZC-D

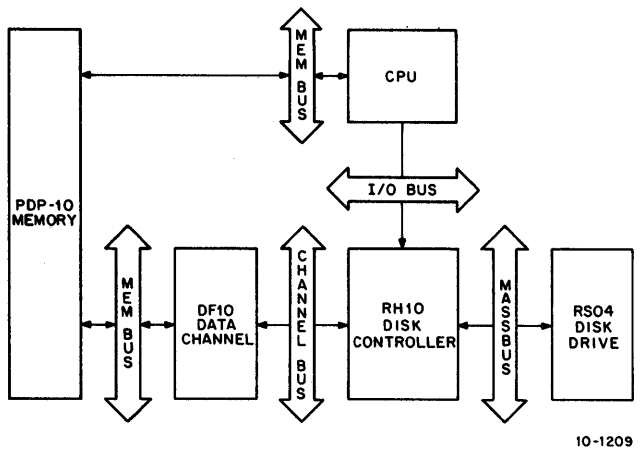


Figure 1-1 RH10 Simplified Block Diagram

Figure 1-3 shows the major RH10 registers employed in a data transfer. In the case of a write data transfer, the data is routed from memory to the RH10 via the DF10. In the RH10, the data is first accepted by the Channel Buffer (CB), transferred to the Assembly Register (AR), and then to the Data Buffer (DB). Note that the Channel Buffer and the Assembly Register are 36-bit registers while the Data Buffer is 18-bits. Therefore, the left-half of the AR is first transferred to the DB which transfers the 18-bits of data to the drive. Then the right half of the AR is loaded into the DB which is then transferred to the drive. For a data transfer read operation, the process is merely reversed, where the data from the drive is transferred to the RH10, to the DF10, and then to memory.

1.3.1 I/O Bus

The PDP-10 I/O Bus is a set of cables which connect all PDP-10 I/O devices to the central processor. Both data and control information flow through the bus which is daisy-chained through each device.

Since all PDP-10 I/O devices share the I/O bus, part of the information carried by the bus indicates which device is to respond. This is accomplished by the device select portion of a PDP-10 input or output instruction which is a 7-bit field [each bit having complementary signals labeled IOS 3 through IOS 9 (refer to Figure 1-4)]. The RH10 is addressed by a device-select of 270_8.

For additional information on the PDP-10 I/O bus, refer to the *DECsystem-10 Interface Manual.*

1.3.2 Memory Bus

The PDP-10 Memory Bus is a set of cables which connect PDP-10 memory modules to the KA10 or KI10 Central Processor, and connects the DF10 Data Channel to memory. Because the PDP-10 processors, the memory modules, and the DF10 are asynchronous, the memory bus is controlled by a request/response scheme, whereby the DF10 issues a request and waits for a response from the memory. Figure 1-5 shows the signals associated with the memory bus. For additional information on the PDP-10 Memory Bus, refer to the DECsystem-10 Interface Manual.

1.3.3 Channel Bus

The channel bus is part of the DF10 Data Channel, which is a high-speed data transfer device that accomplishes direct data transfers between PDP-10 memory and I/O devices such as the RH10 Device Controller. Once enabled, the DF10 functions as an I/O processor and transfers data independently of the program in progress, thereby releasing the central processor for other operations. The program establishes the initial link when it activates the I/O device, which then requests a memory access and primes the data channel to allow the transfer of data when access is granted. Figure 1-6 shows the signals on the DF10 Data Channel. The CHANNEL START, SAWRITE and CHANNEL BUSY signals are synchronous signals which are fed to the logic in each I/O device whereas the other signals are merely bussed in and out of each device. For additional information on the channel bus, refer to the DF10 Data Channel Maintenance Manual.

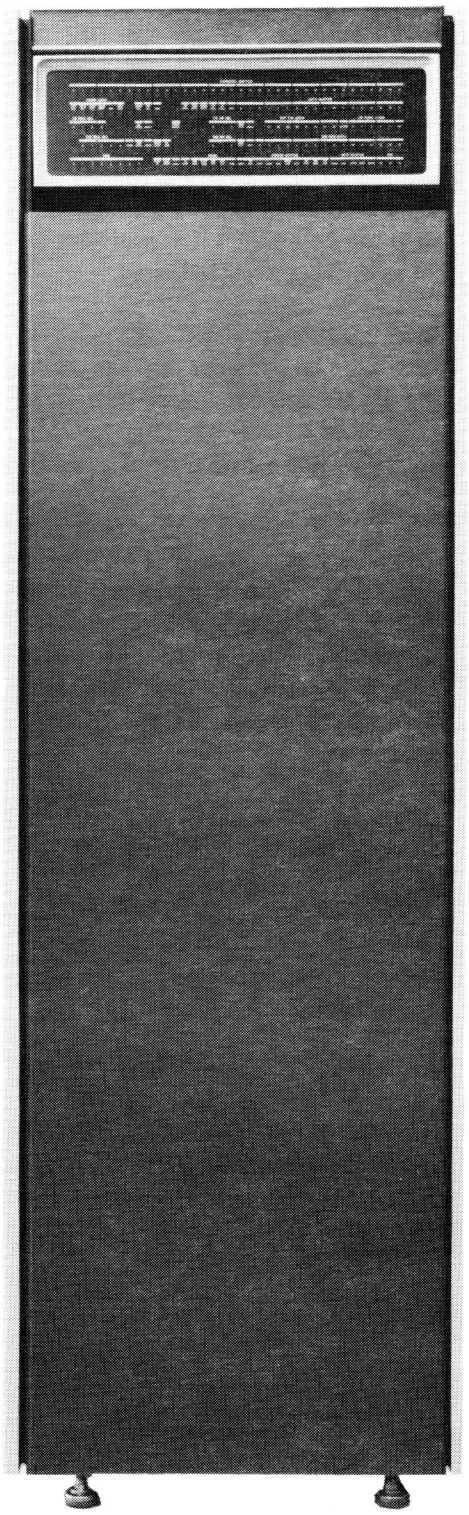


Figure 1-2 RH10 Massbus Controller

1.3.4 Massbus

The Massbus is the name of the interface between the RH10 Controller and the RS04 Disk File. The Massbus provides a parallel data path between the RH10 and the disk device. It has a maximum cable length of 120 ft, allowing 15 ft between drives, if the daisy-chain configuration with a maximum of 8 disks is employed. The Massbus is comprised of two sections: an asynchronous control bus and a synchronous data bus.

The purpose of the asynchronous control bus is to:

a. Transmit control commands and information from the Controller to the drive

b. Notify the Controller when an unusual (attention) condition exists in one or more drives

c. Transmit status information from the drive to the Controller

d. Provide a master reset to all drives from the Controller.

The purpose of the synchronous data bus is to transmit blocks of data at high speed between the Controller and drives and to control the initiation and termination of block transmissions.

1.4 RH10 DEVICE CONTROLLER

The RH10 Controller, in conjunction with a drive such as the RS04, provides an extremely fast and reliable mass storage system that can be employed on time-sharing or real-time data storage applications.

Basic functions performed by the RH10 are:

Write and Read Data Transfers

The basic steps in performing read or write data transfers are:

a. The PDP-10 issues a DATAO instruction with a device select code of 270_8 which specifies the RH10 (Figure 1-7).

b. The contents of the effective address of the DATAO 270_8 instruction is placed on the I/O bus, and contains information as to the drive selected, the DF10 Initial Control Word Address, and the type of operation (read or write).

c. This information on the I/O bus is clocked into the RH10 Control register.

d. DF10 Data Channel is turned on to gain access to memory.

e. When the DF10 responds, a Control bus cycle will be initiated. This cycle will transfer the read or write function code from the RH10 Control register into the addressed drive's Control register.

f. When the Control bus cycle is terminated, the Controller will initiate the data transfer.

g. The data transfer terminates when word count overflow occurs in the DF10 which, in turn, causes the RH10 and the drive to terminate operation.

Write and Read RH10 Registers

The PDP-10 can write or read an RH10 register via the I/O bus.

The procedure for writing a register is as follows:

a. The PDP-10 issues a DATAO instruction with a device select code of 270_8 specifying the RH10. The contents of the effective address specified in this instruction is placed on the I/O bus. This information contains the RH10 register address, the data to be written into the register and a write bit set, denoting a write operation. This bit is bit 06 on the I/O bus and is designated Load Register bit.

b. The data on the I/O bus is clocked into the RH10 register specified in the address bits.

The procedure for reading an RH10 register is as follows:

a. The PDP-10 issues a DATAO instruction with a device select code of 270_8 specifying the RH10. The contents of the effective address specified in this instruction is placed on the I/O bus. This information contains the RH10 register address and the Load Register bit (bit 06) negated. Negation of this bit specifies a read operation.

b. The PDP-10 issues a DATAI instruction with a device select code of 270_8 to transfer the contents of the RH10 register to the I/O bus.

NOTE

The function of placing a DATAO on the I/O bus with Load Register bit 06 on a 0 is merely to store the register address in the Controller, in order that the information be read from the correct register on a succeeding DATAI instruction. This step can be omitted if a 'read after write' of an RH10 register is desired.

Writing or Reading a Drive Register

The PDP-10 can write or read drive registers via the I/O bus, the RH10, and the Massbus (see Figure 1-8).

The procedure for writing a drive register is as follows:

a. The PDP-10 issues a DATAO instruction with a device select code of 270_8 specifying the RH10. The contents of the effective address of this instruction is placed on the I/O bus. The information includes the drive selected, drive register selected, the Load Register bit (bit 06 asserted on I/O bus) and the 16 bits of data to be written.

b. The information on the I/O bus is loaded into the Drive Interface Buffer (DIB).

c. A Massbus control bus cycle is initiated and the data from the DIB is transferred via the Massbus asynchronous bus to the specified register in the drive selected.

The procedure for reading a drive register is as follows:

a. The PDP-10 issues a DATAO instruction with a device select code of 270_8 specifying the RH10. The contents of the effective address of this instruction is placed on the I/O bus. The information contains drive selected, drive register selected, and the Load Register bit negated (bit 06 on the I/O bus).

b. The information on the I/O bus is loaded into the DIB.

c. A Massbus control bus cycle is initiated and the data from the drive register is transferred to the RH10 DIB register via the Massbus asynchronous bus.

d. The PDP-10 issues a DATAI instruction with a device select code of 270_8 to transfer the contents of the RH10 register to the I/O bus.

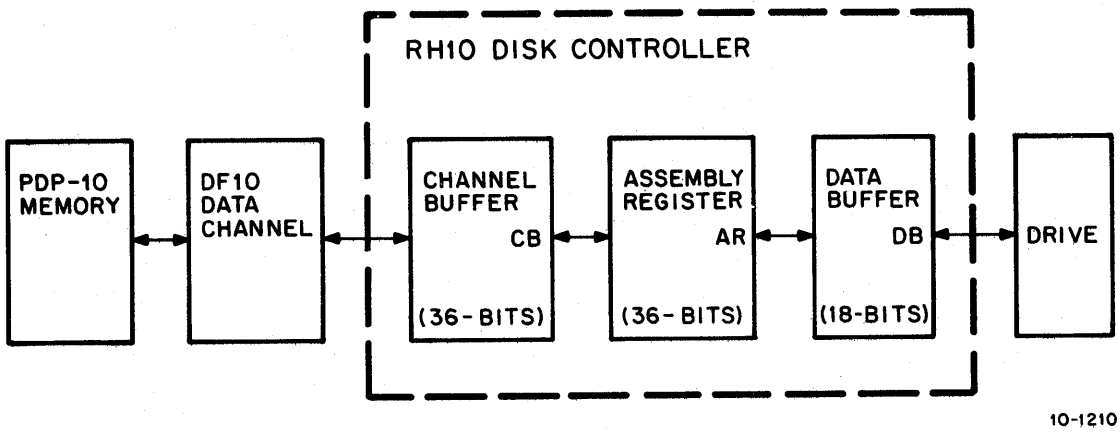


Figure 1-3 RH10 Simplified Data Path Diagram

DR SPLIT

can be used by Device to prevent Processor From Doing RD/PAUSE/WRT operations. Processor Splits RD/PAUSE/WRT IOP Into A READ Followed By A WRITE. This SIGNAL IS NOW used by DEC Controllers But CAN Be Wired In such as wiring "Controller Busy" To THIS SIGNAL Pin on Bus.

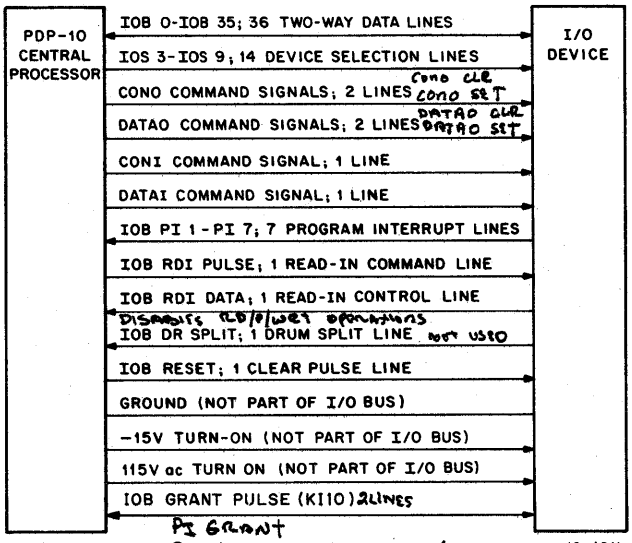


Figure 1-4 I/O Bus Information Flow

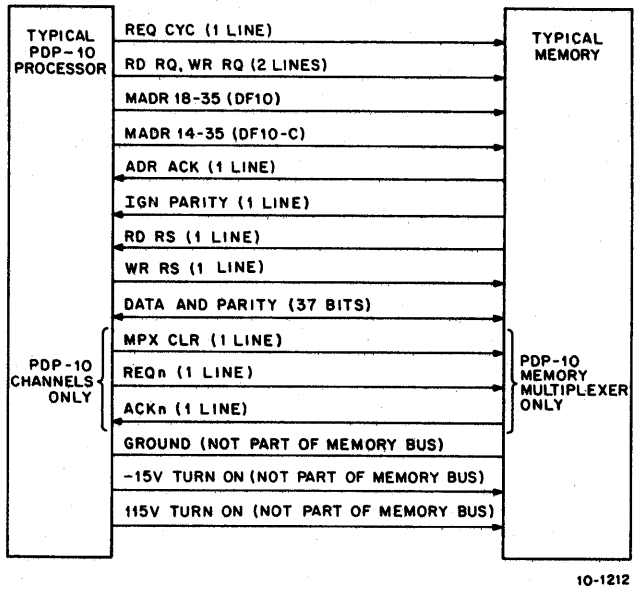


Figure 1-5 Memory Bus Information Flow

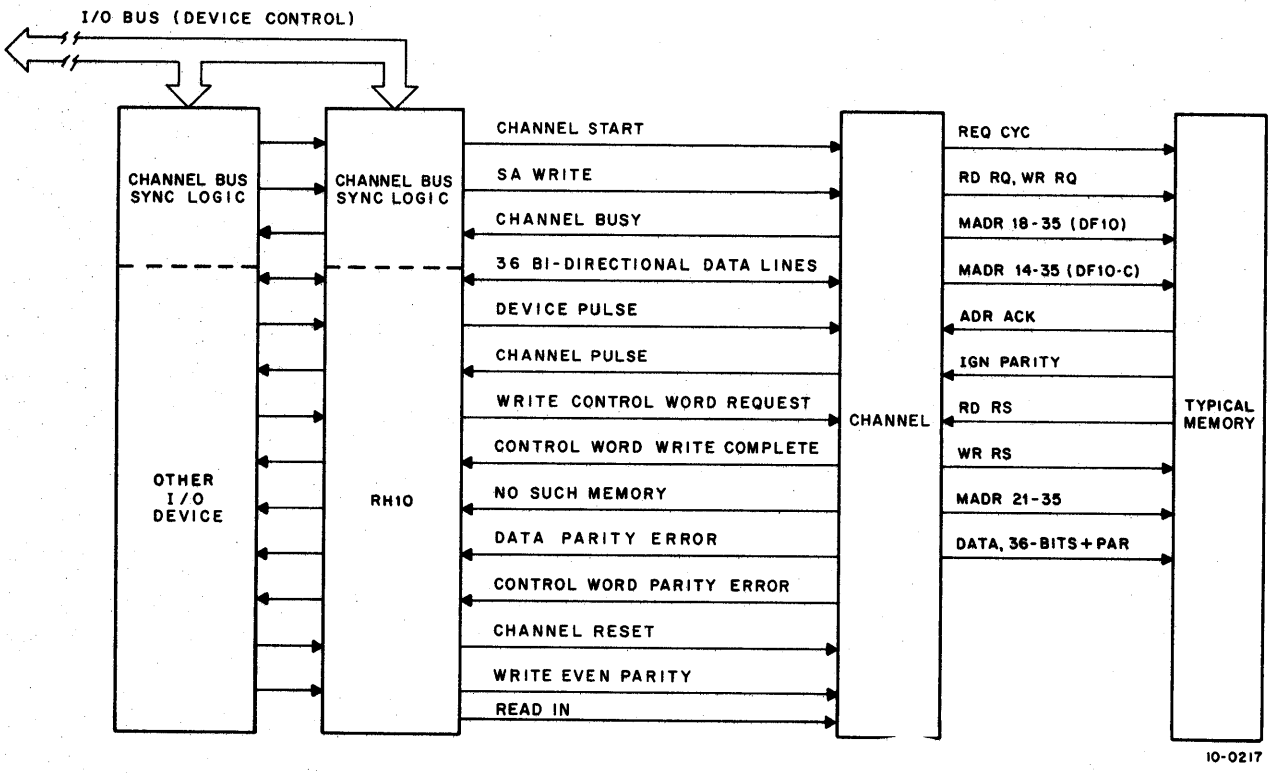


Figure 1-6 DF10 Interface

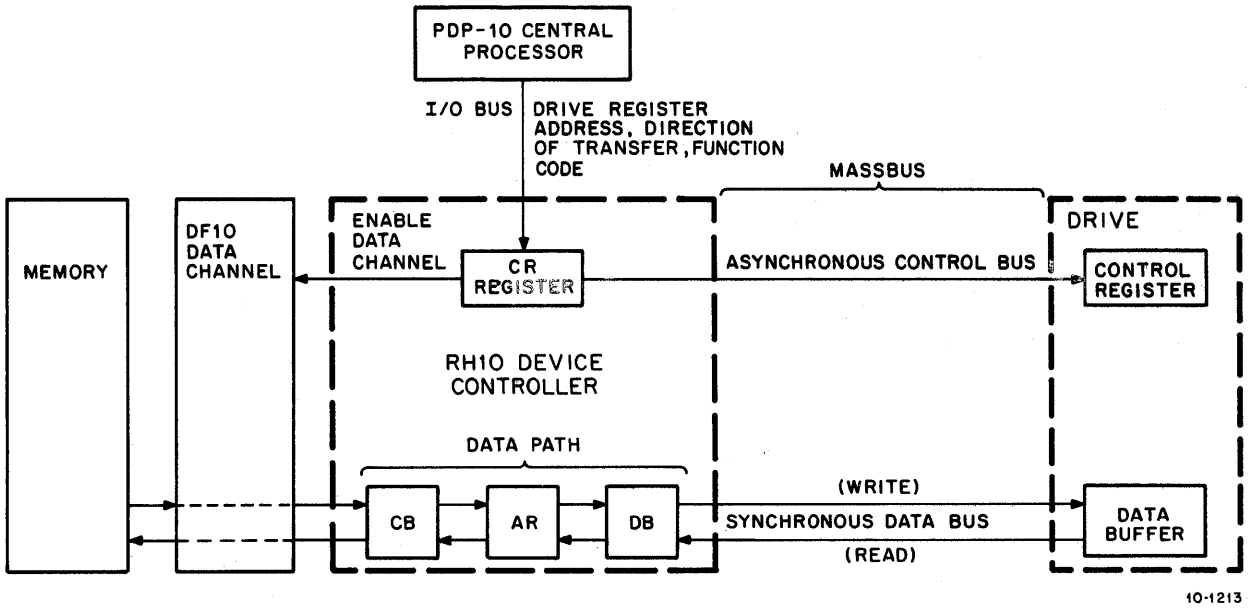


Figure 1-7 Read or Write Data Transfer Diagram

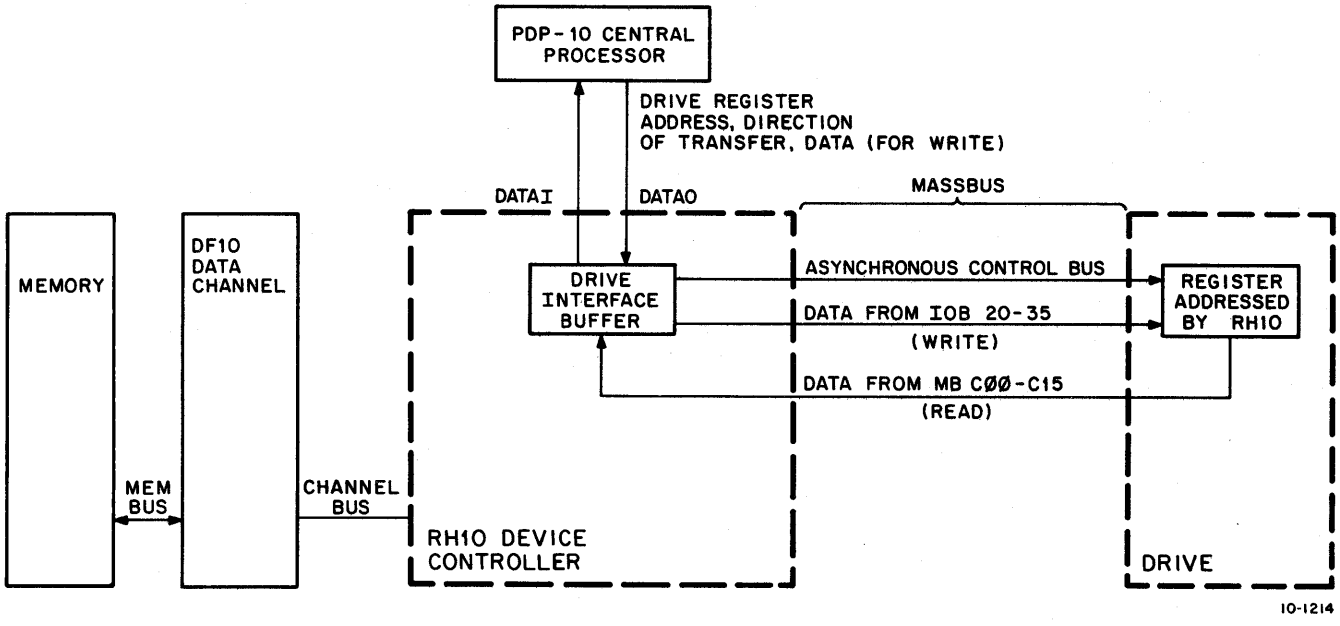


Figure 1-8 Reading or Writing Drive Registers

CHAPTER 2
MASSBUS INTERFACE

2.1 GENERAL

The Massbus provides the interface between the RH10 Controller and the RS04 Disk Files. The Massbus cable can be up to 120 feet in length and up to eight drives may be connected in a daisy-chain configuration. The Massbus consists of two sections – a Data Bus section and a Control Bus section. These buses are described in the following paragraphs.

2.2 DATA BUS

The Data Bus section of the Massbus consists of a 19-bit (18 data bits plus parity bit) parallel data path and six control lines (see Figure 2-1).

Parallel Data Path – The parallel data path consists of an 18-bit data path and an associated parity bit. The data path is bidirectional and employs odd parity. Data is transmitted synchronously, using a clock generated in the drive.

RUN – After a data transfer command has been written into the Control register of the drive, the drive connects to the Data Bus. The Controller then asserts the RUN line to initiate the function. At the end of each sector on the trailing edge of the EBL (End-of-Block) pulse, RUN is strobed by the drive. If it is still asserted, the function continues for the next sector; if it is negated, the function is terminated.

Occupied (OCC) – This signal is generated by the drive to indicate "Data Bus Busy". As soon as a valid data transfer command is written into a drive, and the command is accepted, the drive asserts OCC. Various errors may cause a drive to be unable to execute a command. The Controller will time out in these cases due to no assertion of OCC, and the DBTO (Data Bus Timeout) error will be set in the Controller. OCC is negated at the trailing edge of the last EBL pulse of a transfer.

End-of-Block (EBL) – This signal is asserted by the drive for one word time (1.8 μs) at the end of each sector (after the last SCLK pulse). For certain error conditions, where it is necessary to terminate operations immediately, EBL is asserted prior to the normal time. The data transfer is terminated prior to the end of the sector in this case.

Exception (EXC) – This signal is asserted when an error condition occurs in the drive. The drive will assert this signal to indicate an error during a data transfer command. Once asserted by a drive, the EXC line remains asserted until the trailing edge of the last EBL pulse.

Sync CLK (SCLK), Write CLK (WCLK) – These signals are the timing signals used to strobe the data in the Controller and/or in the drive. During a read operation, the Controller strobes the data lines on the negation of SCLK and the drive changes the data on the assertion of SCLK. During a write operation, the Controller receives SCLK and echoes it back to the drive as WCLK. Consequently, on the assertion of WCLK, the drive strobes the data lines and on the negation of WCLK, the Controller changes the data on the data lines.

2.3 CONTROL BUS

The Control Bus section of the Massbus consists of a 17-bit (16 bits plus parity) parallel control and status path, and 14 control lines (see Figure 2-1).

Parallel Status and Control Path – The parallel status and control path consists of a 16-bit parallel path designated C00 through C15 and an associated parity bit (CPA). The control and status path is bidirectional and employs odd parity.

Drive Select DS (2:0) – These three lines transmit a 3-bit binary code from the Controller to select a particular drive. The drive responds when the (unit) select switch in the drive corresponds to the transmitted binary code.

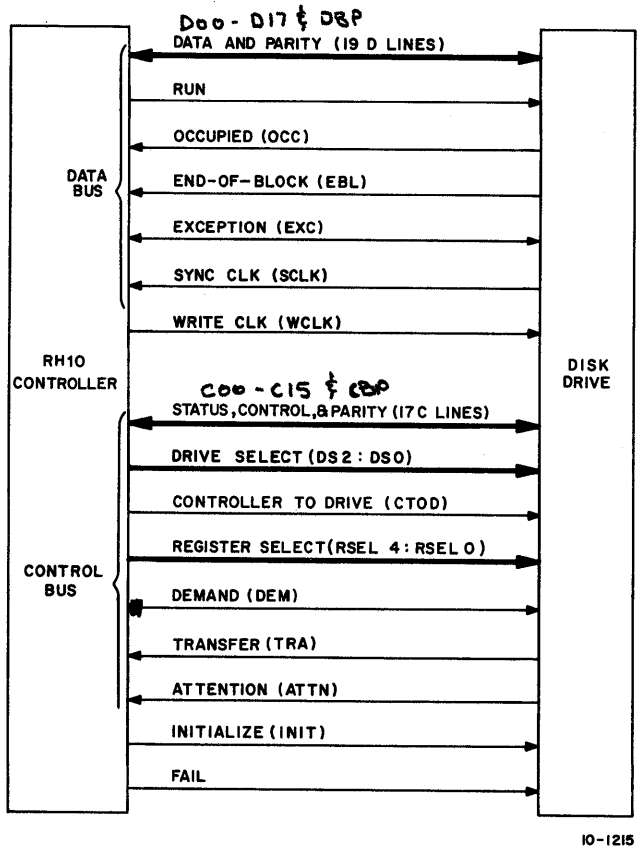


Figure 2-1 Massbus Interface

Controller to Drive (CTOD) – This signal is generated by the Controller and indicates the direction in which data is to be transferred. For a Controller-to-drive transfer, the Controller asserts CTOD. For a drive-to-Controller transfer, the Controller negates this signal.

Register Selects RS (4:0) – These five lines transmit a 5-bit binary code from the Controller. The binary code selects one of the eight drive registers.

Registers	Mnemonic	Addr
Drive Control register	DRCR	00_8
Drive Status register	DRSR	01_8
Drive Error register	DRER	02_8
Drive Maintenance register	DRMR	03_8
Drive Attention Summary register	DRAS	04_8
Drive Desired Address register	DRDA	05_8
Drive Type register	DRDT	06_8
Drive Look Ahead register	DRLA	07_8

NOTE

The two most significant lines (RS4 and RS3) are not used to select registers in the RS04. If these lines are asserted, an Illegal Register (ILR) error occurs.

Demand (DEM) – This signal is asserted by the Controller to indicate that a transfer is to take place on the Control Bus. For a Controller-to-drive transfer, DEM is asserted by the Controller when data is present and settled on the Control bus. For a drive-to-Controller transfer, DEM is asserted by the Controller to request data and is negated when the data has been strobed off the Control bus. In both cases, the RS, DS, and CTOD lines are generated and allowed to settle before assertion of DEM.

Transfer (TRA) – This signal is asserted by the drive in response to DEM. For a Controller-to-drive transfer, TRA is asserted when the data is strobed and is negated when DEM is removed. For a drive-to-Controller transfer, TRA is asserted when the data is asserted on the bus and negated when the negation of DEM is received.

Attention (ATTN) – This line is shared by all 8 drives attached to a Controller; it may be asserted by any drive as a result of an abnormal condition or status change in the drive. The ATA status bit in each drive is set whenever that drive is asserting the ATTN line. ATTN may be asserted due to any of the following conditions:

a. An error while no data transfer is taking place (asserted immediately)

b. Completion of a data transfer command if an error occurred during the data transfer

c. Completion of a non-data transfer command (such as a Search)

The ATA bit in a drive may be cleared by the following actions:

a. Asserting INIT (affects all 8 drives)

b. Writing a 1 into the Attention Summary register (in the bit position for this drive). This clears the ATA bit; however, the error remains set.

c. Writing a Drive Clear command into the Control register (with the GO bit set). Note that clearing the ATA bit of one drive does not always cause the ATTN line to be negated, because other drives may also be asserting the line.

NOTE

There are three cases in which ATA is not reset when a Drive Clear command is written into the Control register (with the GO bit set): (a) if there is a Control Bus Parity error on the write, (b) if an error was previously set, or (c) if an illegal function code (ILF) is written.

Initialize (INIT) – This signal is asserted by the Controller to perform a system reset of all the drives. It is asserted by the Controller on power up or when Controller Reset is generated by a CONO instruction. When a drive receives the INIT pulse, it immediately aborts the execution of any current command and performs all actions described for the Drive Clear command.

Fail – When asserted, this signal indicates a power-fail condition has occurred in the Controller. In particular, this blocks the INIT and DEM signals at the drive and prevents spurious signals from the M5904 Controller transceivers from destroying data on the drives.

2.4 COMMAND INITIATION

Commands are of two types – data transfer commands (read, write) and non-data transfer commands (drive clear, search). Data transfer commands are initiated through the RH10 Control register. All other non-data commands to the register are illegal and will result in an Illegal Op Code error. Non-data transfer commands to a drive are initiated through the Drive Interface Buffer (DIB) and if a read/write function code to this register occurs, it will result in an Illegal Command error.

2.4.1 Non-Data Transfer Commands

Non-data-transfer commands have effect only on the state of the drive. The Controller merely writes the command word (with GO bit set) into the drive Control register. At the completion of the command execution, the drive typically asserts the ATTN line in order to signal its completion.

If the non-data transfer command code written into the drive is not recognized by the drive as a valid command, the drive will immediately signal an error by asserting the ATTN line. The Illegal Function (ILF) error is set.

2.4.2 Data Transfer Commands

To initiate a data transfer command in a drive, the RH10's Control register is loaded via a DATAO instruction which causes a word to be written into the selected drive's Control register (00). The word contains a data transfer command function code in bits 30–34 and a GO bit in bit 35. The GO bit is set when initiating a command. If the command specified is valid, the drive which has been addressed by the program executes the command.

When the data transfer command has been loaded into the RH10 Control register with the appropriate command function code, the DF10 is started and a Massbus Control bus cycle is initiated. The RH10 asserts DEM, the drive returns TRA. The RH10 then asserts RUN and the drive responds with OCC on the data bus portion of the Massbus. It is over this bus that the data transfer will occur. The drive then issues SCLK signals causing the data to be transferred to or from the specified drive.

When the data transfer command has been loaded into the RH10 Control register, the DF10 is started and the data transfer command function code (with the GO bit set) is written into the drive Control register. The drive will respond with TRA and the Controller will assert the RUN line. The drive will then respond by asserting the OCC line. The drive asserts SCLK which causes the data to be transferred to or from the specified drive.

If an error occurs in a drive during a data transfer command, the drive asserts the Exception (EXC) line. This line remains asserted until the trailing edge of the last EBL pulse. If CR DXES is reset, the RH10 Controller will negate the RUN line when it detects EXC and EBL asserted, so that the data transfer is terminated at the end of the sector in which the error was detected. If CR DXES is set, then the data transfer will continue until the end of the specified transfer or until a data bus timeout occurs, depending on the error condition. The drive will continue the transfer for a Class A failure (non-fatal) or terminate immediately for a Class B (fatal) error resulting in a data bus timeout.

2.5 MASSBUS PHYSICAL DESCRIPTION

The Massbus consists of 56 signals including data, control, status and parity. These signals are routed between the RH10 and the drives by 3 40-conductor flat cables. Since Massbus signal transmission (with exception of the FAIL signal) is accomplished by differential transmitter/receiver pairs, each cable can accommodate 20 differential signals. To transfer the 56 signals, 3 20-pair cables are required. On the drive end, the cables are plugged into M5903 Massbus Drive Transceiver cards. On the Controller end, each cable plugs into a M5904 Massbus Controller Transceiver card.

CHAPTER 3
PROGRAMMING

3.1 GENERAL

The RH10 will perform the following basic functions:

Provide the programmer with the capability to directly access drive registers (read or write).

Initiate data transfers upon command, synchronizing the transfer to the DF10 and the associated command list.

Provide maintenance personnel with a means of local control to facilitate debugging and to aid in corrective maintenance procedures.

This chapter describes the register accesses and initiation of data transfers from a programming standpoint. In addition, the bit format and descriptions of the various RH10 registers are provided. The local control for facilitating debugging and corrective maintenance is provided in Chapter 6.

3.2 DRIVE REGISTER ACCESSES

The programmer can read or write a drive register via the Drive Interface Buffer in the RH10, using the DATAO/DATAI format described in Paragraph 3-9.

An address (register select code) of 00–37 specifies a drive register. Addresses greater than 37_8 are used to address registers in the RH10.

NOTE

When a DATAO is issued, the register to be addressed is stored in the Controller and determines the information read back to the CPU on succeeding DATAI's. For example, a DATAO selecting the Interrupt Address register (44_8) would allow the programmer to read this register on all DATAIs that follow until another register is selected by a DATAO. A drive register address ($00–37_8$), when stored, will enable the Drive Interface Buffer (DIB) to be read by the DATAI. The DIB will contain the contents of the drive register, as buffered in the Controller, as well as the address of the drive and drive register accessed on the previous DATAO.

3.2.1 Writing a Drive Register

To write a drive register, a DATAO with Load Register (bit 06) set to 1 causes the data in bits 20–35 to be transferred over the asynchronous control bus to the selected drive (bits 15–17) and loaded in the selected drive register (bits 00–05).

3.2.1.1 Register Access Error (RAE) – If an error is detected in the Controller as a result of the Drive Register Access, one of eight flags in the RAE register (see Paragraph 3.8) will be set where each flag corresponds to a drive address. REGISTER ACCESS ERROR (CONI, bit 29) is the "OR" of the eight RAE flags and will be asserted causing the following to occur provided RAE INTERRUPT ENABLE (CONO, bit 29) had been set prior to the drive register access:

a. An interrupt will occur on the assigned PI channel.

b. All drive register access requests (DATAO $00–37_8$) following the error will be blocked by the hardware. This is done so that the drive and drive register address which resulted in the error will be latched in the DIB register and can be read with a DATAI.

Clearing RAE INTERRUPT ENABLE (CONO, bit 29 = 0) disables the interrupt generated by the error and restores normal operation of the DATAO $00–37_8$. To clear the RAE error condition itself requires a DATAO to the RAE register. RAE is *not* cleared by the Controller when a data transfer is initiated.

If a data transfer is initiated (DATAO 40_8) to a drive for which an RAE had occurred, the Controller will terminate immediately setting DONE, SELECTED DRIVE RAE (CONI bit 10) and ILLEGAL COMMAND (CONI bit 24).

ILL COMM = SD RAE V ILF

This will happen regardless of the state of RAE INTERRUPT ENABLE.

Register access errors which may take place as a result of the register write are as follows:

a. Control Bus Timeout (DATAI, bit 07) – Indicates the drive register access. This error would occur if:

   1. The drive does not exist
   2. The drive is powered down.

b. Illegal Command (DATAI, bit 10) – This error will be set if a read or write function code appears in a register write to a drive's Control register. The register write will take place but the GO bit will not be transmitted to the drive by the RH10. This inhibits the initiation of a data transfer command via the DIB register.

It should be noted that the RAE flag (CONI) will not be raised (even though an RAE condition exists) unless the interrupt enable bit (CONO) is set.

3.2.1.2 Drive Error – If an error is detected in the drive as a result of the register write, an error flag will set in the drive's ERROR register and the Attention line on the Massbus will be asserted. The Attention will generate an interrupt on the assigned channel if CXR ATTN EN is set.

Generate Even Control Bus Parity (bit 18 of the DATAO) is provided so that bad parity may be generated on the Control bus during a register write. This will be used by the diagnostic programmer to verify operation of the drive's parity checker circuits and will cause a drive error.

3.2.1.3 Notes to Programmer –

1. A register write should not be initiated to a drive doing a read or write operation except when the drive is in maintenance mode. In this case, a transfer is single-stepped by writing the MAINTENANCE register. Writes to other registers will result in a drive error and the data transfer in progress will be aborted. (A write to the Attention Summary register is permissible.)
2. If a register write is issued to a read-only drive register, no error will be indicated, CBTO will not be set, and the register data will be ignored (not loaded) by the drive.

3.2.2 Reading Drive Register

To read a drive register, a DATAO with Load Register (bit 06) set to ZERO causes the selected drive (bits 15–17) to gate the contents of the selected register (bits 00–05) onto the asynchronous Control bus. The register contents are then strobed and stored in the RH10 DIB register. The programmer would follow the DATAO with a DATAI to read the register contents (bits 20–35).

3.2.2.1 Register Access Error – Errors which cause a Register Access Error for the drive register read are as follows:

a. Control Bus Timeout (DATAI, bit 06) – Also occurs for a register write. (See Paragraph 3.2.1.1.)

b. Control Bus Parity Error (DATAI, bit 08) – Indicates incorrect parity detected by the Controller on the asynchronous Control bus.

c. Data Late (DATAI, bit 09) – Sets on the DATAI following a DATAO $00–37_8$ if the drive register access initiated by the DATAO has not completed. It indicates invalid register data. Data Late errors can occur because there is a contention between the program initiated DATAO $00–37_8$ and the hardware initiated Control register write associated with the DATAO 40_8. (The cycle occurs on a DF10 response that is asynchronous with respect to the DATAO.) This means that, in the worst case, two drive register accesses must occur in one I/O bus cycle time. The timing problem is further compounded if the RH10 is operated on the KI10 I/O bus. To ensure errorless operation, the programmer should introduce a 3 μs stall between the DATAO $00–37_8$ and the DATAI.

The action of Register Access Error and the function of RAE Interrupt Enable are as described for the drive register write. (See Paragraph 3.2.1.1.)

Generate Even Control Bus Parity (DATAO, bit 18) may be used by the diagnostic programmer to cause a Control Bus Parity Error for the drive register read. It causes the polarity of parity generated by the drive to be inverted as it is received by the Controller from the Massbus. Thus, it

forces a parity error and would be used to verify the parity checking circuits in the Controller. Note that Control Bus Parity, the state of the Massbus Parity line itself, may be read directly by a DATAI (bit 19).

3.2.2.2 **Drive Error** – If an error is detected in a drive as a result of the register read, an error flag will set in the drive's Error register and the Attention line on the Massbus will be raised. The action of Attention and Attention Enable are as described for the drive register write (see Paragraph 3.2.1.2).

NOTE

There are no programming restrictions for drive register reads. Barring hardware failure, any existing drive register may be read at any time without causing a drive error.

3.2.3 Control Bus Overrun

If a drive register access is initiated (DATAO $00–37_8$) and the previous drive register access has not completed, Control Bus Overrun (CONI, bit 28) will set causing an interrupt and blocking any further DATAO's to the RH10. A data transfer in progress will complete normally. The error condition can only be cleared by resetting Control Bus Overrun with a CONO, bit 29 = 1. The reasons for this error occurring are the same as explained for Data Late error (see Paragraph 3.2.2.1). The programmer should insert 3 μs stalls between consecutive drive register accesses to ensure errorless operations.

3.3 INITIATING DATA TRANSFERS

Prior to initiating a data transfer, the DF10 command list must be stored in memory and the starting surface address must have been loaded in the drive. A DATAO addressed to the RH10 Control register (Controller Register Select = 40_8) with Load Register (bit 06) = 1 will initialize the RH10, start the DF10 and initiate the data transfer to or from the selected drive (bits 15–17) by causing the Controller to write the drive's Control register directly. If the RH10 is already busy, the DATAO 40_8 is ignored.

The DF10 Initial Control Word Address is contained in bits 21–28. Write Even Memory Parity (bit 29) is provided to allow operation of the parity checking circuits in the DF10 to be verified. Generate Even Data Bus Parity (bit 18) performs a similar function and allows the drive's data bus parity checker to be checked for a write operation and allows the Controller's parity network to be verified for a read operation. The direction of data transfer, that is, read or write, is specified by bits 30–35 and includes a Function Code & GO bit. This corresponds to the Function Code & GO bit shown in the format for a drive's Control register, and it is these bits that are written in the drives Control register by the RH10 to start the transfer.

NOTE

Only function codes for a read or write should be used in the DATAO 40_8. A code for another operation such as NO-OP or Drive Clear will result in an Illegal Command Error (CONI, bit 24), causing the RH10 to set DONE and produce immediate termination. Operations other than read or write should be initiated by writing the drives Control register directly with a drive register write (see Paragraph 3.2.1). The GO bit (bit 35) may be considered as part of the Function code and should always be a 1. If the GO bit is Zero, the RH10 Control register will be loaded but no further action will take place. No error flag will be raised.

Maintenance Mode (bit 11) is provided for diagnostic purposes. In this mode, the RH10 disconnects from the Massbus and may be single-stepped with the DATAO 50_8. (See Paragraph 3.6.)

Disable Transfer Error Stop (DXES, bit 19) is provided so that certain errors will not abort data transfers. This is useful for software error recovery routines. Errors disabled are Channel Data Parity Error, detected by the DF10 during a drive write operation, Data Bus Parity Error, detected by the RH10 during a drive read operation and a drive Exception error indication detected during a read or write operation.

Termination and Interrupts – When the RH10 is initialized by the DATAO 40_8, it will start the DF10 Data Channel unless the following error conditions are detected:

ERROR CONDITIONS	RH10 STATUS FLAG
RH10 dc voltages are out of tolerance.	Power Supply Fail (CONI, bit 25)
Data transfer attempted to a drive for which a Register Access Error was detected previously.	Selected Drive RAE (CONI, bit 10) Illegal Command (CONI, bit 24)
Function Code (bits 30–34) other than for a read or write operation.	Illegal Function Code (CONI, bit 09) Illegal Command (CONI, bit 24)

If the above errors are detected, the RH10 terminates immediately setting DONE and raising an interrupt on the assigned PI channel. With no errors detected and the DF10 started, the Controller will write the drive's Control register and will start a data transfer in the drive unless the following errors are detected. As for above, errors will cause the RH10 to terminate immediately, setting DONE and causing an interrupt.

ERROR CONDITIONS	RH10 STATUS FLAG
Drive failed to respond to Control register write request indicating drive does not exist or is powered down.	Drive Response Error (CONI, bit 23) Control Bus Timeout (DATAI, bit 07)
An error was detected in the drive as a result of writing the drive's Control register. Errors which might occur are Illegal Function Code, Illegal Desired Block Address Set Previously, Write Attempted to Write-Locked Track, etc.	Exception (CONI, bit 19)

NOTE

When the drive terminates after asserting Exception, Attention will be raised on the Massbus (CONI, bit 30) and will cause an RH10 interrupt if Attention Enable (CONO, bit 30) had been set.

Drive failed to take control of synchronous bus as evidenced by the OCC line not being asserted after the Control register write request. This would occur if the drive cannot perform the data transfer due to an error resulting from the Control register write or because of a previous error.	Drive Response Error (CONI, bit 23) Data Bus Timeout (DATAI, bit 08)

NOTE

A condition which could cause the Drive Response Error occurs when the DATAO 40_8 had been issued to a drive in which a previous error had not been cleared by the programmer. This condition arises since a drive shall enter the "Clear Required" state after experiencing any error. In this state, a function code will be loaded but GO will not be set. In order to set GO, the drive error must first be cleared either by writing 0s into the Error register, writing a Drive Clear code in the Control register, or asserting INIT on the Massbus.

With the Function Code and GO set in the drive and no errors detected, a data transfer will be started in the drive. Normal termination occurs when the DF10 fetches a Zero control word. If a read operation is performed, the RH10 will read through to the end of the current data block, with CRC or ECC being checked by the drive, before setting DONE. Errors which may occur during a data transfer and which cause an abnormal termination are listed below.

ERROR CONDITIONS	RH10 STATUS FLAG
Memory Bus Parity Error detected by DF10 during control word fetch.	Channel Error (CONI, bit 20) Control Word Parity Error (CONI, bit 16)
Memory failed to respond to memory cycle request by DF10.	Channel Error (CONI, bit 20) Non-Existent Memory (CONI, bit 17)

NOTE

In both cases above, where the DF10 terminates the Controller, the RH10 behaves as in normal termination except that error flags will be on with DONE when the Controller terminates. In the cases below, the RH10 initiates the termination in the following ways:

RH10 dc voltages are out of tolerance. The DF10 and RH10 are shut down immediately. A data transfer in progress may continue to the end of the current data block. This flag cannot be cleared as long as the error condition exists.	Power Supply Fail (CONI, bit 25)
If the channel does not transfer data fast enough, the RH10 shuts down the DF10 and terminates at the end of the current data block as for a normal termination. That is, blocks are zero-filled from the point of overrun on a write and ECC or CRC are checked on a read.	Overrun (CONI, bit 22)
If a Memory Bus Parity Error is detected in the DF10 for data being written on the drive and the error is not disabled (DXES = 0), the channel is shut down immediately. The RH10 terminates at the end of the current data block, the word with the error will not be written and it and all words following in the block will be replaced with zeros. ECC or CRC will be written by the drive.	Channel Error (CONI, bit 20) Channel Data Parity Error (CONI, bit 15)

(continued on next page)

ERROR CONDITIONS	RH10 STATUS FLAG
If a parity error is detected by the RH10 on the synchronous data bus during a read operation and the error is not disabled (DXES = 0) the DF10 is shut down immediately and the RH10 terminates at the end of the current data block after ECC or CRC is read by the drive. The word in error is not transferred to memory.	Data Bus Parity Error (CONI, bit 18)
If a drive error occurs, and the error is not disabled (DXES = 0), the DF10 is shut down immediately. If the drive error is a Class A error, the Controller terminates at the end of the current sector as for a normal termination. If a Class B, or catastrophic type error occurs, the Controller terminates immediately with a write or read shutting down immediately, possibly within the data block. If the error is disabled (DXES = 1), the DF10 is not shut down and the RH10 will not terminate for Class A errors but will terminate for Class B errors. Termination occurs not due to Exception (disabled by DXES = 1) but due to Drive Response Error which occurs when the drive drops its OCC line on shutting down.	Exception (DXES = 0) (CONI, bit 19) Drive Response Error (DXES = 1) (CONI, bit 23)
A CONO with STOP (bit 31) on a ONE will shut down the DF10 and RH10 immediately. A data transfer in progress in the drive would continue to the end of the current sector block.	BUSY = 0; DONE = 1

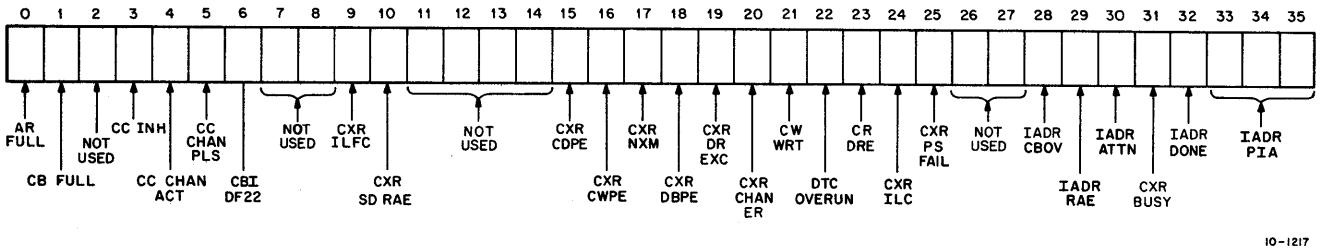


Figure 3-1 CONI Instruction – Bit Format

3.4 CONO/CONI INSTRUCTIONS

The bit format for the CONI is shown in Figure 3-1; Table 3-1 provides a description of each bit. The bit format for the CONO is shown in Figure 3-2; Table 3-2 provides a description of each bit.

3.5 CONTROL REGISTER

A DATAO to the control register is DATAO 40_8. The bit format for the DATAO 40_8 is shown in Figure 3-3; Table 3-3 provides a description of each bit. The bit format for the Control register DATAI 40_8 is shown in Figure 3-4; Table 3-4 provided a description of each bit.

Table 3-1
CONI Instruction – Bit Definitions

Bit	Designation	Description
0	AR Full	AR Full when set, indicates that the Assembly Register (AR) is full with 36 bits of data. During a write, contents of AR is transferred to the DB when the DB is empty. During a read, contents of AR is transferred to CB when CB is empty.
1	CB Full	CB Full, when set, indicates that the Channel Buffer (CB) is full with 36 bits of data. During a write, contents of CB is transferred to AR when AR is empty. During a read, contents of CB is transferred to DF10 when DF10 issues CHAN PLS in response to last DEV PLS sent by the RH10.
2	Not Used	
3	CC INH (CC Inhibit)	CC INH disables CHAN START OUT TO DF10 causing the RH10 to disconnect from DF10. This occurs during termination sequences.
4	CC CHAN ACT (Channel Active)	CHAN ACT, when asserted, indicates that the RH10 can request the DF10 Data Channel. Remains set for the whole data transfer and is cleared when the RH10 terminates.
5	CC CHAN PLS (Channel Pulse)	When CHAN PLS is asserted during a write data transfer (write onto disk), it is accompanied by a data word for transfer to the RH10. When CHAN PLS is asserted during a read data transfer (read from disk), the DF10 is ready to accept a word from the RH10. Cleared By DEV PLS
6	CBI DF22	DF22 indicates that the RH10 is connected to a 22-bit data channel (DF10-C with 22 bits of memory address). The DF10 is an 18-bit data channel (18 bits of memory address).
7,8	Not Used	
9	CXR ILFC (Illegal Function Code)	Only a read or write function code (71_8 or 61_8) is to be stored in the CR register in the RH10. If some code other than these is detected, the ILFC bit is raised.
10	CXR SD RAE (Selected Drive Register Access Error)	SD RAE is raised when a drive which has been selected has previously asserted a Register Access Error.
11–14	Not Used	

Table 3-1 (Cont)
CONI Instruction – Bit Definitions

Bit	Designation	Description
15	CXR CDPE (Channel Data Parity Error)	CDPE is asserted when a word transferred from memory to the DF10 has a parity error. The DF10 sends the CDPE signal to the RH10, indicating bad parity.
16	CXR CWPE (Control Word Parity Error)	CWPE is asserted when a control word fetched from memory has a parity error when it was checked in the DF10. This signal causes the DF10 to terminate, and causes the RH10 to terminate as a result of CC INH.
17	CXR NXM (Non-Existent Memory)	NXM is sent to the RH10 to indicate that the DF10 has addressed a non-existent memory or that the addressed memory location has not responded. This results in termination by the data channel and causes the RH10 to terminate as a result of CC INH.
18	CXR DBPE (Data Bus Parity Error)	DBPE is set during a read operation when the data from the drive has been transferred to the RH10 and a parity error has been computed.
19	CXR EXC (Exception)	EXC indicates an error condition has been asserted in the drive during a data transfer. This line stores the EXC condition.
20	CXR CHAN ER (Channel Error)	CHAN ER is the OR of Channel Data Parity Error, Control Word Parity Error, and Non-Existent Memory and merely presents a programming convenience to indicate an error condition with the single bit.
21	CXR CW WRT (Control Word Written)	When CW WRT is asserted, it indicates that the control word has been written into memory by the DF10. This control word was written via a CONO instruction with bit 21 on a 1 (WRITE CW). It allows the programmer to determine where the program is when executing a data transfer.
22	DTC OVERRUN	When OVERRUN is set during a write, it indicates that the DF10 did not supply a word to the RH10 in time for the next SCLK from the drive. During a read, it indicates that the drive is transferring words faster than the DF10 can accept them.
23	CR DRE (Drive Response Error)	DRE represents the OR of Data Bus Timeout or Control Bus Timeout. It is set upon initiation of a data transfer via bits 7 or 8 of the Control register in the RH10.

BITS 18-35 used IN CONI SKIP INSTRUCTIONS

Table 3-1 (Cont)
CONI Instruction – Bit Definitions

Bit	Designation	Description
24	CXR ILC (Illegal Command) BIT 9 BIT 10	ILC is the OR or Illegal Function Code (ILFC) and Register Access Error in the selected drive (SD RAE).
25	CXR PS FAIL	PS FAIL, when asserted, indicates that the dc low voltage detector has detected a dc low condition which sets the PS FAIL flip-flop.
26,27	Not Used	
28	DIB CBOV (Control Bus Overrun)	CBOV is set when the control bus is overrun. This occurs when an attempt to start a DIB cycle is made before the completion of the last DIB cycle.
29	IADR RAE Interrupt enable is Set (Register Access Error)	RAE EN is set by bit 29 of the CONO instruction and, when set, allows a Register Access Error (CONI, bit 29) to interrupt.
30	IADR ATTN Interrupt enable is Set (Attention)	ATTN EN is set by bit 30 of the CONO instruction and, when set, allows the Attention condition (CONI, bit 30) to interrupt.
31	CXR BUSY	BUSY indicates that the RH10 is busy doing data transfer and is not used during register accesses.
32	CXR DONE	DONE, when set, indicates that a data transfer has just completed, either normally or due to an error condition.
33	IADR PIA (Priority Interrupt Address)	Indicates the state of the priority level flip-flops. These levels are assigned by the PDP-10 and allow the peripheral device to interrupt on its assigned level.

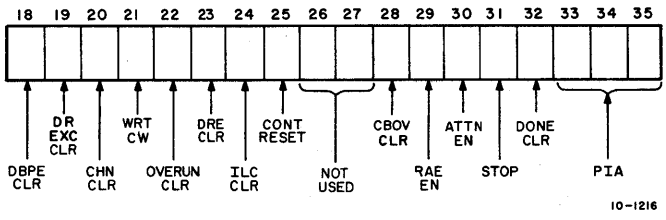


Figure 3-2 CONO Instruction – Bit Format

E,E → DEVICE

E in 18-35 is Duplicated in 00-17 and the complete word is sent as E,E Dec. Devices only use E IN RIGHT HALF 18-35

Table 3-2
CONO Instructions – Bit Instructions

Bit	Designation	Description
18	DBPE CLR (Data Bus Parity Error Clear)	Setting this bit clears the CXR DBPE flip-flop.
19	EXC CLR (Exception Clear)	Setting this bit clears the CXR DR EXC flip-flop.
20	CHAN ER CLR (Channel Error Clear)	Setting this bit clears the CXR CHAN ERR condition.
21	WRT CW (Write Control Word)	Setting this bit allows the DF10 to write a control word into memory. This word can be used to determine the portion of a data transfer that has been completed.
22	OVERRUN CLR	Setting this bit clears the DTC OVERRUN flip-flop.
23	DRE CLR (Drive Response Error Clear)	Setting this bit clears the CR CBTO and CR DBTO flip-flops.
24	ILC CLR (Illegal Command Clear)	Setting this bit clears the ILFC and SD RAE flip-flops.
25	CONT RESET (Controller Reset)	Setting this bit clears all error flip-flops. This is equivalent to I/O bus reset.
26,27	Not Used	
28	CBOV CLR (Control Bus Overrun Clear)	Setting this bit clears the DIB CB OVERRUN flip-flop.
29	RAE EN (Register Access Error Enable)	Setting this bit enables the RAE logic to interrupt the central processor.
30	ATTN EN (Attention Enable)	Setting this bit allows an Attention condition raised in the RH10 to interrupt the central processor.
31	STOP	Setting this bit causes the RH10 to clear CXR BUSY, set CXR DONE, releases the DF10 and stops the data transfer.
32	DONE CLR	Setting this bit direct resets the DONE flip-flop.
33–35	PIA (Priority Interrupt Address)	A 3-bit priority interrupt address.

Table 3-3
RH10 Control Register DATAO – Bit Definitions

Bit	Designation	Description
0–5	Controller Register Select (40_8)	A 6-bit code specifying the RH10 Control Register.
6	LR (Load Register)	For register addresses $00–37_8$, specifies a transfer of information from the Controller to the drive when equal to ONE and specifies a transfer from the drive to the Controller when equal to ZERO. For addresses greater than 37_8 and when equal to ONE, specifies that the Controller register will be loaded with the contents of the DATAO. When equal to ZERO, the register will not be loaded. Thus, with Controller registers and LR = 0, a means is provided to select a register to be read on the next DATAI without altering the register's contents.
7–10	Not Used	
11	Maint Mode (Maintenance Mode)	This bit, when set, will disconnect the RH10 from the Massbus. It allows simulated data transfers in conjunction with the DATAO 50_8 and allows for testing of Massbus interface error conditions.
12–14	Not Used	
15–17	CR DR SEL 00–02 (Drive Select Bits)	A 3-bit code used to specify 1 of 8 possible drives connected to the Massbus.
18	CR GEN EVD (Generate Even Parity on the Data Bus)	Allows the drives data bus parity checker to be checked for a write operation and allows the Controller's parity network to be verified for a read operation.
19	CR DXES (Disable Transfer Error Stop)	DXES is provided so that certain errors will not abort data transfers. The errors which may be disabled are: 1. Channel Data Parity Error (detected by the DF10 during a drive write operation) 2. Data Bus Parity Error (detected by the RH10 during drive read operation) 3. Drive Exception Error (detected during a read or write operation).
20	Not Used	
21–28	CR INAD 27 THRU 34 (Initial Control Word Address)	An 8-bit code specifying the address of the initial control word in core memory.

Table 3-3 (Cont)
RH10 Control Register DATAO – Bit Definitions

Bit	Designation	Description
29	CR WTEVM (Write Even Memory Parity)	Allows operation of the parity checking circuits in the DF10 to be verified.
30–34 35	CR FUNC CODE 00 THRU 04 GO Bit	A 5-bit function code used to specify a read or write data transfer and includes a GO bit (bit 35). The function code and GO bit corresponds to the function code and GO bit in the drives Control register. These bits are written into the drives Control register by the RH10 to initiate the data transfer.

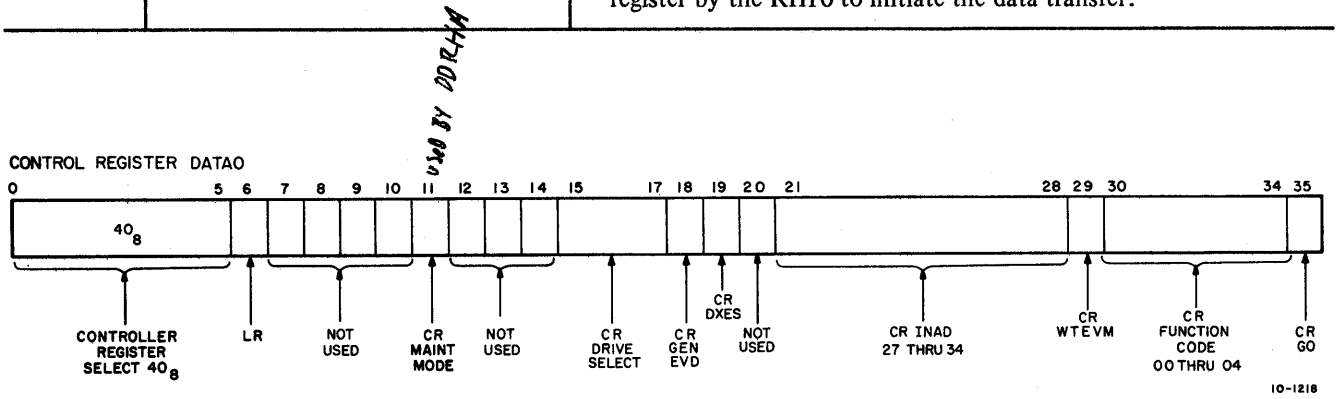


Figure 3-3 RH10 Control Register DATAO Bit Format

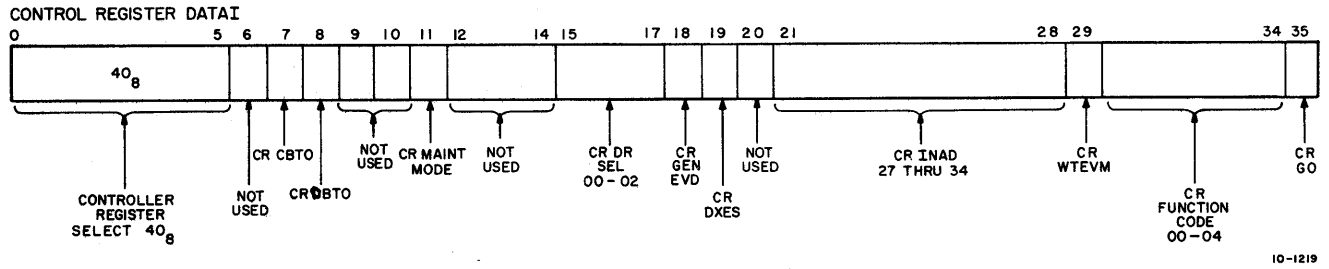


Figure 3-4 RH10 Control Register DATAI – Bit Format

Table 3-4
RH10 Control Register DATAI – Bit Definitions

Bit	Designation	Description
0–5	Controller Register Select (Control Register = 40_8)	A 6-bit code specifying the RH10 Control register.
7	CR CBTO (Control Bus Timeout)	Indicates that the drive did not respond to the drive register access. This error would occur if: 1. The drive does not exist or, 2. The drive does not respond. 1.5 µS MAXIMUM BETWEEN DEMAND & TRANSFER.
8	CR DBTO (Data Bus Timeout)	Indicates that the drive did not respond with OCC (occupied) within 10 ms after the assertion of RUN.
9,10	Not Used	
11	CR Maint Mode (Maintenance Mode)	Indicates to the programmer that the RH10 has been placed in the Maintenance Mode.
12–14	Not Used	
15–17	CR DR SEL 00–02 (Drive Select Bits)	A 3-bit code which indicates 1 of 8 possible drives which have been selected.
18	CR GEN EVD (Generate Even Parity on Data Bus)	Indicates that even parity generation is enabled for the synchronous data bus.
19	CR DXES (Disable Transfer Error Stop) *	Indicates that the DXES bit has been set.
20	Not Used	
21–28	CR INAD 27 THRU 34 (Initial Control Word Address)	Indicates the initial control word address set in by the DATAO 40_8 instruction.
29	CR WTEVM (Write Even Memory Parity)	Indicates that the DF10 has been enabled to write even parity into memory. THIS IS OVERRIDDEN BY A SWITCH CALLED "WRITE EVEN PARITY LOCKOUT".
30–34	CR FUNC CODE 00–04	Indicates the function code specified by the DATAO 40_8 instruction.
35	GO	Indicates the state of the GO bit.

* DXES
1. CHANNEL DATA PE IGNORED
2. IGNORE DATA BUS PAR ERRORS ON DEVICE READS
3. IGNORE EXE ERRORS ON READ OR WRITE

3.6 DATA BUFFER REGISTER

A DATAO to the Data Buffer register is DATAO 50_8. Figure 3-5 shows the bit format for the DATAO 50_8; Table 3-5 provides a description of each bit. Figure 3-6 shows the bit format for the Data Buffer register DATAI; Table 3-6 provides a description of each bit.

The main functions of the DATAO 50_8 are:

1. To provide a means of loading a data pattern in Local mode from the switch panel prior to initiating a write.

2. To provide a means of single-stepping a data transfer in Maintenance Mode. In this mode with a DATAO 40_8 having been issued, a DATAO 50_8 with bit 07 (DIAG SCLK) on a 1 will generate a simulated SCLK. If the data transfer is a read, bits 17–35 will be loaded in the Data Buffer at that time, simulating read data and parity from the drive. This, in turn, will allow 36 bits of data to be assembled in the AR register and transferred to memory if the data channel is enabled. If the data transfer is a write operation and the data channel is enabled, the simulated SCLK will cause the data from the AR to be loaded into the data buffer thus allowing data to be transferred from memory.

3. Allows loading and testing of the data buffer directly from the I/O bus.

Being able to read the Data Buffer register with a DATAI becomes useful during error recovery routines. Since the register is not loaded after a data bus parity error occurs (with DXES = 0), the erroneous data pattern can be read and logged.

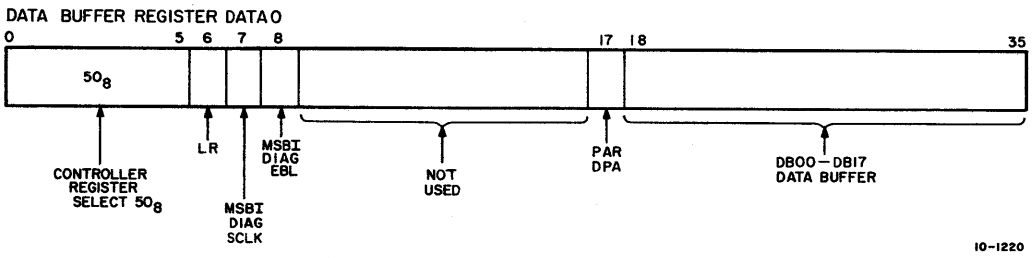


Figure 3-5 RH10 Data Buffer DATAO – Bit Format

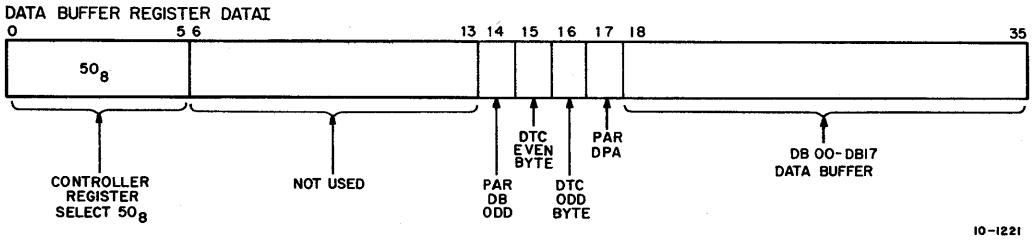


Figure 3-6 RH10 Data Buffer DATAI – Bit Format

Table 3-5
RH10 Data Buffer DATAO – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (Data Buffer = 50_8)	A 6-bit code specifying the Data Buffer register in the RH10.
6		For register addresses $00–37_8$, specifies a transfer of information from the Controller to the drive when equal to ONE and specifies a transfer from the drive to the Controller when equal to ZERO. For addresses greater than 37_8 and when equal to ONE, specifies that the Controller register will be loaded with the contents of the DATAO. When equal to ZERO, the register will not be loaded. Thus, with Controller registers and LR = 0, a means is provided to select a register to be read on the next DATAI without altering the register's contents.
7	MSBI DIAG SCLK (Diagnostic Sync Clock)	When the RH10 is in Maintenance Mode (via assertion of bit 11 in the DATAO 40_8 instruction), bit 07 of the DATAO 50_8 will generate a simulated SCLK to provide a means of single-stepping a data transfer.
8	MSBI DIAG EBL (Diagnostic End of Block)	When the RH10 is in Maintenance Mode (via assertion of bit 11 in the DATAO 40_8 instruction), bit 08 of the DATAO 50_8 will generate a simulated EBL pulse to provide a means of termination.
9–16	Not Used	
17	PAR DPA (Data Bus Parity)	Provides a means to simulate data bus parity and would be used mainly by the diagnostic programmer in conjunction with GEN EVD (DATAO 40_8, bit 18) to verify the parity checking circuits in the RH10.
18–35	DB 00 THRU 17 (Data Buffer, 18 Bits)	A DATAO 50_8 with Load Register bit 6 = 1 loads bits 18–35 into the 18-bit data buffer in the RH10. The data buffer holds the data received by a drive during a read operation and the data to be written during a write operation. In normal operation, this register may not be loaded by the DATAO 50_8 if the RH10 is doing a transfer (BUSY = 1). The DATAO is ignored in this case.

Table 3-6
RH10 Data Buffer DATAI – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (Data Buffer – 50_8)	A 6-bit code specifying the Data Buffer register in the RH10.
6–13	Not Used	
14	PAR DB ODD	Indicates that the data in the data buffer and the parity bit on the data bus is computed odd.
15	DTC Even Byte	Indicates the even (upper) byte of the 36-bit data word has been loaded into the Data Buffer on a write operation.
16	DTC Odd Byte	Indicates the odd (lower) byte of the 36-bit data word has been loaded into the Data Buffer on a read or write operation.
17	PAR DPA	Denotes the state of the parity bit on the synchronous Massbus.
18–35	DB 00–17 (Data Buffer)	Stores the 18 bits of data from the drive on a read operation or stores the data to be written during a write operation. The data buffer can be read by issuing a DATAI 50_8 and is useful during error recovery routines.

3.7 INTERRUPT ADDRESS REGISTER

The Interrupt Address register allows for storage of an interrupt vector address for KI10-type interrupts. The KI10 interrupt bit (bit 16) is provided to enable this mode of operation. If bit 17 = 0, a normal KA10 interrupt will be generated. The Interrupt Address Register is selected by a Controller register select code of 44_8. A DATAO 44_8 loads bits 18–35 of the I/O bus into bits 18–35 of the Interrupt Address register. Figure 3-7 shows the bit format of the DATAO 44_8; Table 3-7 provides a description of each bit. Figure 3-8 shows the bit format of the DATAI 44_8; Table 3-8 provides a description of each bit.

3.8 REGISTER ACCESS ERROR (RAE) STATUS REGISTER

The RAE register contains eight error flags that are used to store register access errors which may occur during register read or register write operations. Each flag corresponds to a drive address from 0–7, with one or more errors, which will raise the REGISTER ACCESS ERROR (CONI, bit 29). A DATAO or DATAI to the RAE register is DATAO 54_8 or DATAI 54_8. The DATAO 54_8 is provided to clear the RAE condition. A 1 in the bit position corresponding to each flag will reset that particular flag. Figure 3-9 shows the bit format for the DATAO 54_8 while Table 3-9 provides a description of each bit. Figure 3-10 shows the bit format for the DATAI 54_8; Table 3-10 provides a description of each bit.

3.9 DRIVE INTERFACE BUFFER (DIB)

The DIB register is used to perform drive register read and drive register write operations (see Paragraph 3.2). Figure 3-11 shows the DIB DATAO format and Table 3-11 provides a description of each bit. Figure 3-12 shows the DIB DATAI format and Table 3-12 provides a description of each bit.

3.10 CHANNEL BUFFER

The Channel Buffer is a 36-bit storage register which receives 36-bit data words from the DF10 during a write and receives data words from the AR during a read. A DATAO 74_8 will enable the Channel Buffer to be read back on a succeeding DATAI. The channel *cannot* be loaded via the DATAO.

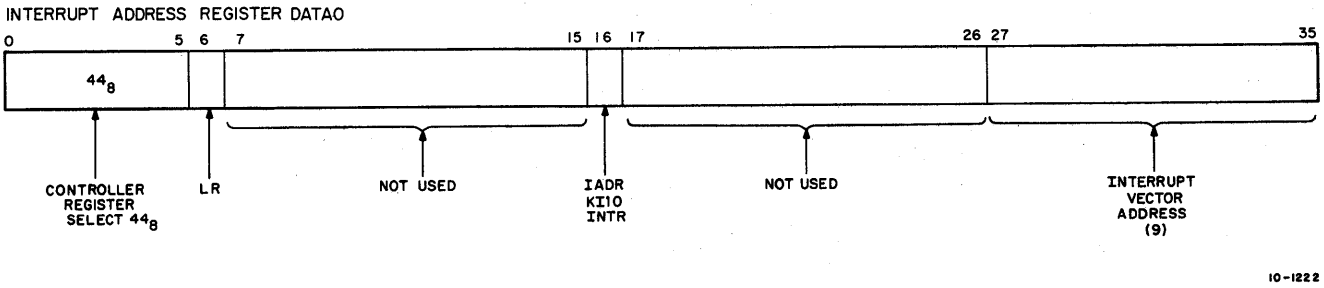


Figure 3-7 RH10 Interrupt Address DATAO – Bit Format

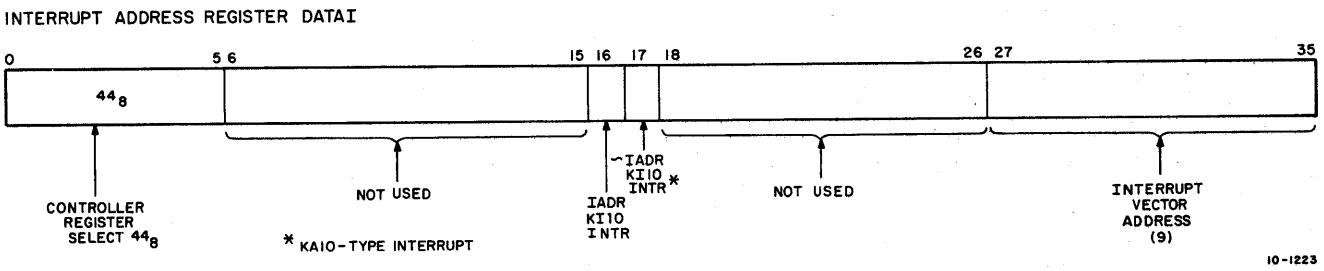


Figure 3-8 RH10 Interrupt Address DATAI – Bit Format

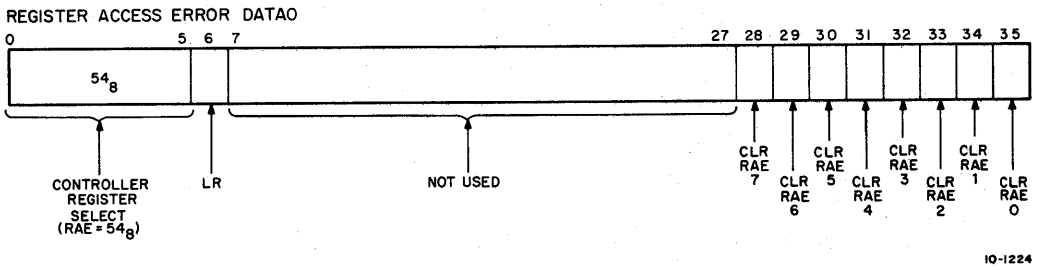


Figure 3-9 Register Access Error DATAO – Bit Format

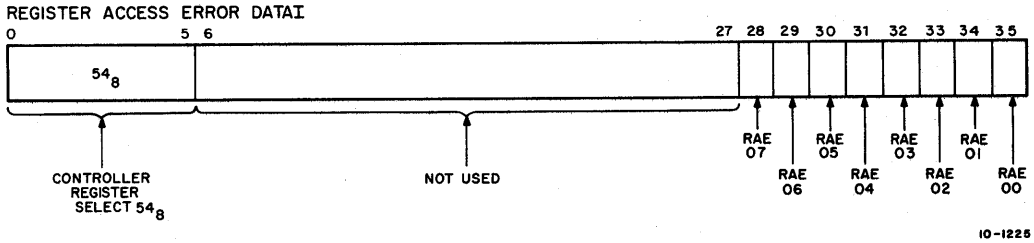


Figure 3-10 Register Access Error DATAI – Bit Format

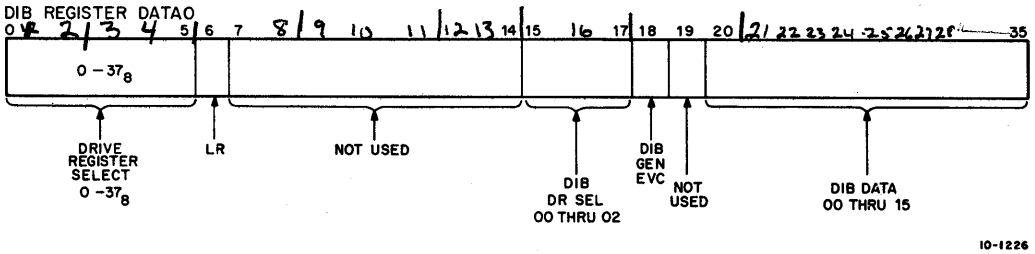


Figure 3-11 DIB DATAO – Bit Format

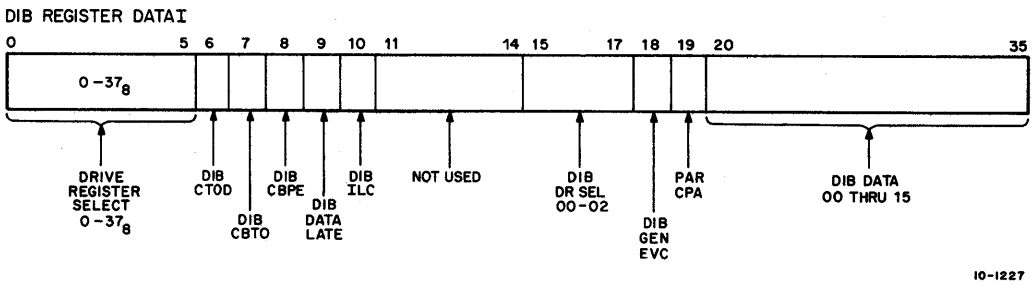


Figure 3-12 DIB DATAI – Bit Format

Table 3-7
Interrupt Address DATAO – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (Interrupt Address = 44_8)	A 6-bit code specifying the Interrupt Address register in the RH10.
6	LR (Load Register)	For register addresses $00–37_8$, specifies a transfer of information from the Controller to the drive when equal to ONE and specifies a transfer from the drive to the Controller when equal to ZERO. For addresses greater than 37_8 and when equal to ONE, specifies that the Controller register will be loaded with the contents of the DATAO. When equal to ZERO, the register will not be loaded. Thus, with Controller registers and LR = 0, a means is provided to select a register to be read on the next DATAI without altering the register's contents.
7–15	Not Used	
16	IADR KI10 INTR	Enables KI10-type interrupts when set and KA10-type interrupts when reset.
17–26	Not Used	
27–35	IADR 27 THRU 35 (Interrupt Vector Address)	Stores a 9-bit vector address from the CPU when doing KI10-type interrupts.

Table 3-8
Interrupt Address DATAI – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (Interrupt Address = 44_8)	A 6-bit code specifying the Interrupt Address register in the RH10.
6–15	Not Used	
16	IADR KI10 INTR	When set, this bit indicates a KI10-type interrupt is specified.
17	IADR KA10 INTR	When set, this bit indicates a KA10-type interrupt is specified.
18–26	Not Used	
27–35	IADR 27 THRU 35 (Interrupt Vector Address)	Displays the 9-bit vector address sent over from the KI10 Processor.

Table 3-9
Register Access Error DATAO – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (RAE = 54_8)	A 6-bit code specifying the RAE register in the RH10.
6	Load Register	For register addresses 00–37_8, specifies a transfer of information from the Controller to the drive when equal to ONE and specifies a transfer from the drive to the Controller when equal to ZERO. For addresses greater than 37_8 and when equal to ONE, specifies that the Controller register will be loaded with the contents of the DATAO. When equal to ZERO, the register will not be loaded. Thus, with Controller registers and LR = 0, a means is provided to select a register to be read on the next DATAI without altering the register's contents.
7–27	Not Used	
28–35	Clear bits	Eight individual clear bits to clear the eight individual RAE flags.

Table 3-10
Register Access Error DATAI – Bit Descriptions

Bit	Designation	Description
0–5	Controller Register Select (RAE = 54_8)	A 6-bit code specifying the RAE register in the RH10.
7–27	Not Used	
28–35	RAE 07 – RAE 00, respectively	Eight individual RAE flags for each of eight possible drives.

Table 3-11
DIB DATAO – Bit Descriptions

Bit	Designation	Description
0–5	Drive Register Select	A 6-bit code specifying 1 of 32 drive registers.
6	LR (Load Register)	For register addresses 00–37_8, specifies a transfer of information from the Controller to the drive when equal to ONE and specifies a transfer from the drive to the Controller when equal to ZERO. For addresses greater than 37_8 and when equal to ONE, specifies that the Controller register will be loaded with the contents of the DATAO. When equal to ZERO, the register will not be loaded. Thus, with Controller registers and LR = 0, a means is provided to select a register to be read on the next DATAI without altering the register's contents.
7–14	Not Used	
15–17	DIB DR SEL 00 THRU 02 (Drive Select)	A 3-bit code used to specify 1 of 8 possible drives.
18	DIB GEN EVC (Generate Even Parity on Control Bus)	Allows even parity to be generated on the control bus portion of the Massbus during a register write and even parity to be received on a read. This will be used by the diagnostic programmer to verify operation of the drive's parity controller and checker circuits.
19	Not Used	
20–35	DIB DATA 00 THRU 15 (Drive Register Data)	With Load Register (bit 6) equal to 1, these bits contain the information to be transferred to the selected register specified by bits 00–05. With bit 6 on a 0, these bits will contain the data read from the drive register by the DATAO.

Table 3-12
DIB DATAI – Bit Descriptions

Bit	Designation	Description
0–5	Drive Register Select	A 6-bit code specifying 1 of 32 drive registers.
6	DIB CTOD (Controller to Drive)	If this bit is a 1, it denotes a write operation and if it is a 0, it denotes a read operation (drive-to-memory).
7	DIB CBTO (Control Bus Timeout)	Indicates that the drive did not respond to the drive register access, either because the drive does not exist or the drive is powered down.
8	DIB CBPE (Control Bus Parity Error)	Indicates incorrect parity detected by the RH10 on the control bus portion of the Massbus.
9	DIB Data Late	Sets on the DATAI following a DATAO $00–37_8$ if the drive register access initiated by the DATAO had not completed. It indicates invalid register data. To prevent errors, the programmer should introduce a 3 μs stall between a DATAO $00–37_8$ and a DATAI.
10	DIB ILC (Illegal Command)	Sets if a read or write function code appears in a register write to the Control register in a drive. The register write will take place but the GO bit will not be transmitted to the drive by the RH10. This ensures that a data transfer can only be initiated in the correct way, i.e., by the DATAO 40_8. If ILC was not implemented, it would be possible for two drives to simultaneously transfer data on the Massbus.
11–14	Not Used	
15–17	DIB DR SEL 00 THRU 02 (Drive Select)	A 3-bit code used to specify 1 of 8 possible drives.
18	DIB GEN EVC (Generate Even Parity on Control Bus)	May be used by the diagnostic programmer to cause a Control Bus Parity Error for the drive register read. It causes the polarity of the parity generated by the drive to be inverted as it is received from the RH10 off the Massbus. Thus, it forces a parity error and would be used to verify the parity checking circuits in the RH10. The state of the Massbus parity line itself may be read directly from a DATAI, bit 19.
19	PAR CPA	Allows the programmer to read the state of the parity line on the Massbus.
20–35	DIB DATA 00 THRU 15 (Drive Register Data)	Stores the contents of the register specified by bits $00–05_8$. For a drive register the register data is contained in bits 20–35.

CHAPTER 4
THEORY OF OPERATION

4.1 GENERAL

This chapter describes the accessing of drive registers, using a simplified flow diagram, to describe the sequence. The chapter also describes the theory of operation for accomplishing read and write data transfers. Figure 4-1 represents a detailed block diagram of the RH10. Interface diagrams are also provided to show the interrelationships between the various system components. Flow diagrams describe the read and write data transfers.

4.2 ACCESSING DRIVE REGISTERS

The RH10 can write or read drive registers by performing a DIB write or a DIB read cycle, respectively. This is accomplished as a result of issuing a DATAO to the RH10 DIB register (address $00–37_8$). Bits 00–05 of this instruction specify one of 32_{10} possible drive registers; bit 06 specifies a write operation when asserted and a read operation when negated, and bits 15–17 designate one of eight selected drives. The DATAO 00 through DATAO 37_8 instruction is associated with the DIB register as all register read and write operations are performed via this register.

4.2.1 DIB Write Cycle

In a DIB write cycle, the DIB register is loaded by the DATAO instruction. This instruction specifies the register selected, the load register bit, the drive selected and the data which is loaded in bits 20–35.

The RH10 then initiates a Massbus control bus cycle to transfer the data from the DIB register to the register specified by the address loaded in the left-half of the DIB register. Figure 4-2 is a simplified flow diagram which shows the major sequence of events for both a DIB write and a DIB read cycle. This paragraph describes the events for a DIB write cycle whereas subsequent paragraphs describe the action for a DIB read cycle.

The DIB write cycle is initiated by a DATAO to the RH10 DIB register ($00–37_8$). If a previous DIB cycle is in progress, an OVERRUN condition is raised and the DATAO instruction is blocked. If no cycle was in progress, a 100-ns delay occurs and the RH10 generates a DIB CLK signal. This signal clocks the address information (specified register, write register operation, and selected drive) into the address portion (left-half) of the DIB register. DIB CLK also causes DIB DATA CLK to be asserted. This signal clocks the data from bits 20–35 of the I/O bus into the data portion (right-half) of the DIB register.

The DIB CLK causes DIB CYC REQ (DIB Cycle Request) to be asserted, indicating a DIB cycle is requested. DIB CYC REQ causes DIB CYC and CYC ACT to be asserted, indicating a DIB cycle has been initiated. This initiates a 275-ns deskew delay which allows settling time for the address information and data at the output of the DIB register. At the end of 275 ns, the RH10 issues a DEM signal which is supplied to the drive via the Massbus. Upon receipt of DEM, the drive strobes the Massbus and gates the data into the selected drive register.

The drive will respond by generating TRA which will generate MSBC END CYC PLS (End Cycle Pulse). This clears the cycle by clearing CYC ACT and clearing DEM.

4.2.2 DIB Read Cycle

In a DIB read cycle, a DATAO is issued to the RH10 DIB register ($00–37_8$) which causes the 16 bits of data in the drive register to be transferred to the DIB register in the RH10. Bits 00–18 of the DATAO instruction specify the drive and register to be read from. The RH10 then initiates a Massbus control bus cycle to transfer the data from the selected drive register to the DIB register.

The DIB read cycle is initiated by issuing a DATAO 00 – DATAO 37_8 instruction. If a previous DIB cycle is in progress, an OVERRUN condition is raised and the DATAO instruction is blocked (Figure 4-2). If no cycle was in progress, a 100-ns delay occurs and the RH10 generates a DIB CLK signal. This signal clocks the address information (specified register, read operation, selected drive) into the address portion of the DIB register. DIB CLK causes DIB CYC REQ to be asserted which, in turn, asserts DIB CYC and CYC ACT indicating a DIB cycle is in progress. After a 275-ns deskew delay, to allow the address information at the DIB register output to stabilize, DEM is issued. The drive, upon receipt of DEM, strobes the Massbus interface and gates the contents of the specified register onto the Massbus along with TRA. Upon receipt of TRA, the RH10 generates a 175-ns read deskew delay to allow time for the data on the Massbus to stabilize. At the end of 175 ns, MSBC LD DIB DATA is asserted which generates DIB DATA CLK. DIB DATA CLK clocks the contents of the Massbus data lines into the DIB register. After a 125-ns delay, MSBC LD DIB DATA DLY is generated. This delay allows parity to be computed on the data. If the parity is even (Parity error), a Control Bus Parity error is raised. The DIB read cycle is terminated by MSBC END CYC PLS, which is asserted as a result of LD DIB DATA DLY.

4.3 WRITE DATA TRANSFER INTERFACE DIAGRAM DESCRIPTION

Figure 4-3 is an interface diagram of the write data transfer and shows the main signals between the memory, DF10, RH10, and drive and also shows the sequence in which they occur. Time is shown vertically with Time 0 at the top.

Initially, the starting address is loaded into a register in the drive. The DATAO 40_8 instruction is then issued, which causes the CR register in the RH10 to be loaded with the drive select bits, initial control word address, and a write function code with the GO bit set (61_8). The CR register (register 0) is automatically addressed when doing a control cycle so it is not necessary to specify the register.

Loading the CR register causes CC ACTIVE BUF in the RH10 to set which, in turn, sets CC CHAN ACTIVE. CC CHAN ACTIVE asserts CHN START OUT to start the DF10 Data Channel. The DF10 receives CHN START OUT and transmits CHN BUSY IN to the RH10, which causes the RH10 to assert CC CHAN SEIZED, indicating that the RH10 has control of the DF10. CC CHAN SEIZED also causes a DEV PLS to be transferred to the DF10 along with the Initial Control Word Address (ICWA). The DF10 strobes the ICWA which is normally a jump instruction to a control word. The diagram shows an initial control word address of 100. The DF10 fetches the contents of location 100 which contains 0, 500. This instruction dictates that the program jumps to location 500.

The DF10 then fetches the contents of location 500 which contains a valid control word of (777775, 1000). This instruction dictates that a two-word write operation is to be performed, starting at location 1000 + 1 (1001). The DF10 issues a READ REQ to fetch the first data word from location 1001. The memory sends this word to the DF10 along with a RDRS (Read Restart) signal. The DF10, in turn, transfers the word to the RH10 along with a CHAN PLS signal. The data word is clocked into the CB register in the RH10. It is then transferred successively to the AR and then to the DB.

NOTE

When the data word is transferred from the CB to the AR, the CB becomes empty and the RH10 sends a DEV PLS to the DF10 requesting another data word.

The CHAN PLS signal from the DF10, in addition to enabling the loading of the data word in the CB, also initiates a Massbus control cycle which causes the function code and GO bit to be written into the selected drives' control register. The cycle is initiated by the RH10 issuing DEM on the Massbus. Upon receipt of DEM, the drive responds with Transfer (TRA). TRA terminates the control cycle and the RH10 initiates the data transfer by issuing RUN. The drive responds with Occupied (OCC) which connects the drive to the synchronous portion of the Massbus. Now, the RH10 waits for SCLK signals from the drive. The SCLK signal from the drive is received by the RH10 and is echoed back as a Write Clock (WCLK) signal. The RH10 places the data on the Massbus on the leading edge of SCLK and the drive strobes the data into its buffer on the trailing edge of SCLK. Consequently, the data word from the DB is transferred to the drive as a result of the first SCLK signal.

To summarize the transfer, the DF10 does a READ RQ to fetch the data word from memory, memory places the data word and RDRS on the bus. The DF10 then strobes the data word and transfers it to the CB register in the RH10 along with a CHAN PLS. The data word is clocked from the CB into the AR, the RH10 issues a DEV PLS to the DF10, requesting another word (when the CB is emptied), and the word in the AR is clocked into the DB. When the drive issues a SCLK (leading edge), the data word in the DB is

RH10 DISK CONTROLLER

I/O BUS

I/O BUS XMTRS

I/O BUS RECEIVERS

IOB

DATAI V PI START

36 BIT DATA

INTERRUPT ADDRESS

I/O BUS MIXER

ISM (I/O STATUS MIXER)

ISM

CB DATA

DIB DATA

RAE DATA

DB DATA

IADR DATA

CR DATA

(CONI)

CXR DATA

SEL IDAR REG DATAI

CONI

DATAO

IOB DATAO

LOCAL DATAO

DATAI
CONO, CONI,
DEV SEL, READ IN

DATA

I/O BUS CONTROL

IBC

INTERRUPT ADDRESS

PI START

PI GRANT

PI REQ SYNC

IOB 0-2

INTERRUPT ADDRESS REGISTER AND CONTROL LOGIC

44 IADR

IOBD 16, 27-35

IBC IADR REG SEL

IBC DATAO SET

IOBD 06

CONTROLLER REGISTER SELECTION LOGIC

REGISTER SELECT DECODER

SEL CR REG 40

SEL IADR REG 44

SEL DB REG 50

SEL RAE REG 54

SEL CB REG 74

CR REG DATA I

IADR REG DATAI

DB REG DATAI

RAE REG DATA I

CB REG DATA I

DATA I

SEL DIB REGISTER DATAI

ENABLE

IBC

CR SEL 01

CR SEL 02

CR SEL 03

CR SEL 00 (1)

CR SEL00 (0)

IBC DATAO CLR

IOBD 00-03

CONTROLLER REGISTER ADDRESS STORAGE

IBC

I/O BUS DATA MIXER

IOBD

SWITCH DATA

MAINTENANCE SWITCH PANEL
LOCAL-IOBD=
SWITCHES
REMOTE-IOBD=
I/O BUS RCVRS SWP

IBC DATAO CLR PLS

~ IOBD 00

DIB CB OVERRUN (0)

DRIVE INTERFACE BUFFER

00-37

DIB

READ/WRITE DRIVE REGISTER
(DIB CYCLE)

TO MASSBUS CONTROL

TO I/O STATUS (ISM)

DATAO 00-37

DATAI 00-37

TO REGISTER ACCESS ERROR

CHANNEL BUS

CHANNEL BUS CONTROL

CONTROL BUS INTERFACE

CBI

CHANNEL CONTROL LOGIC (PERFORMS CHANNEL BUS HANDSHAKE)

CC

START XFR

IBC DATAO SET

IBC CONT REG SEL

DTC XFR COMP

IOBD 06

CONTROL REGISTER

40

CR

TO I/O STATUS (ISM)

DATAO 40

DATAI 40

INITIAL WORD

DATA

CHANNEL BUS DATA XMTRS & RCVRS

CBD

REGISTER DA

C00 - C15 & PARITY

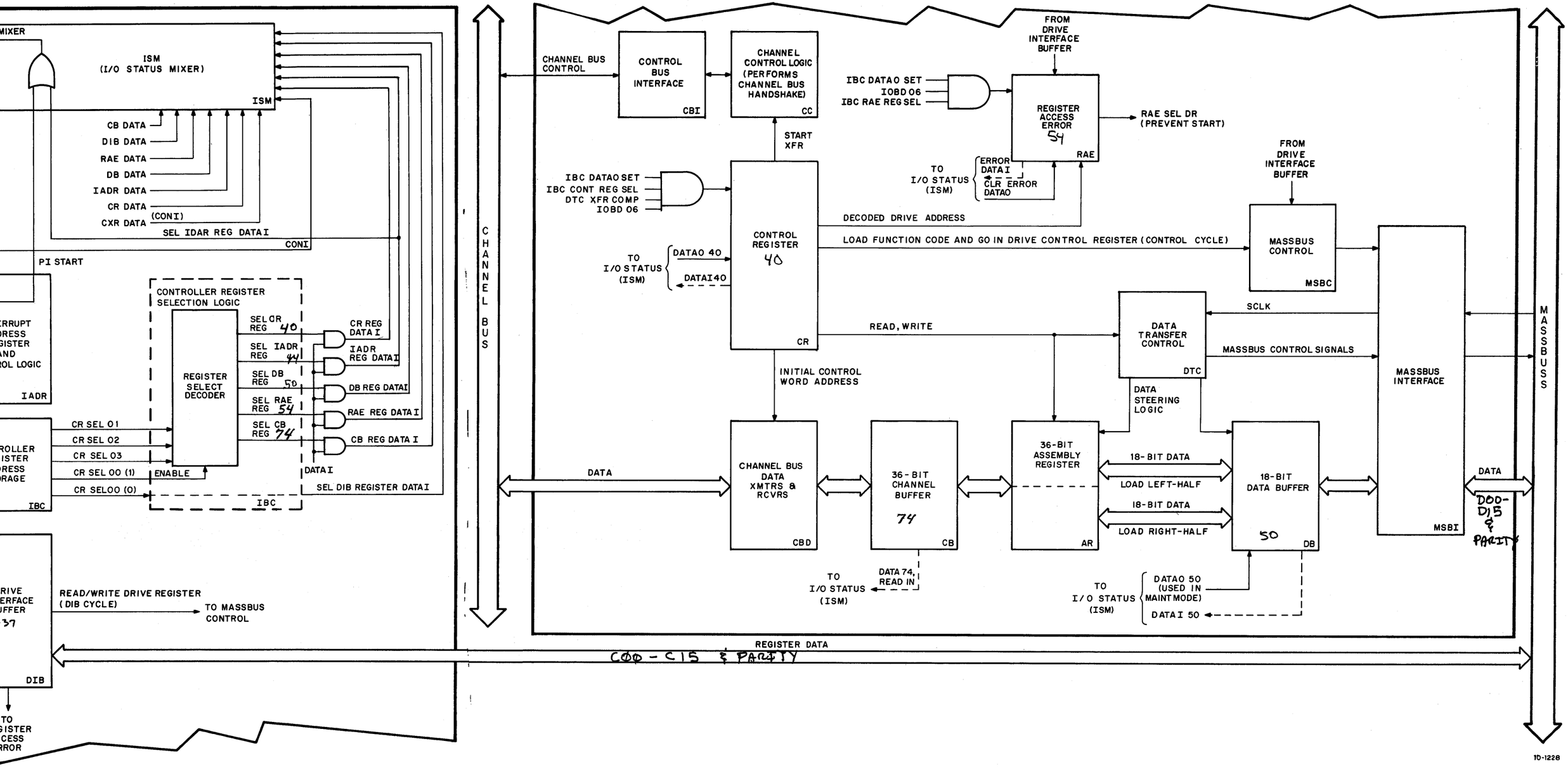


Figure 4-1 RH10 Detailed Block Diagram

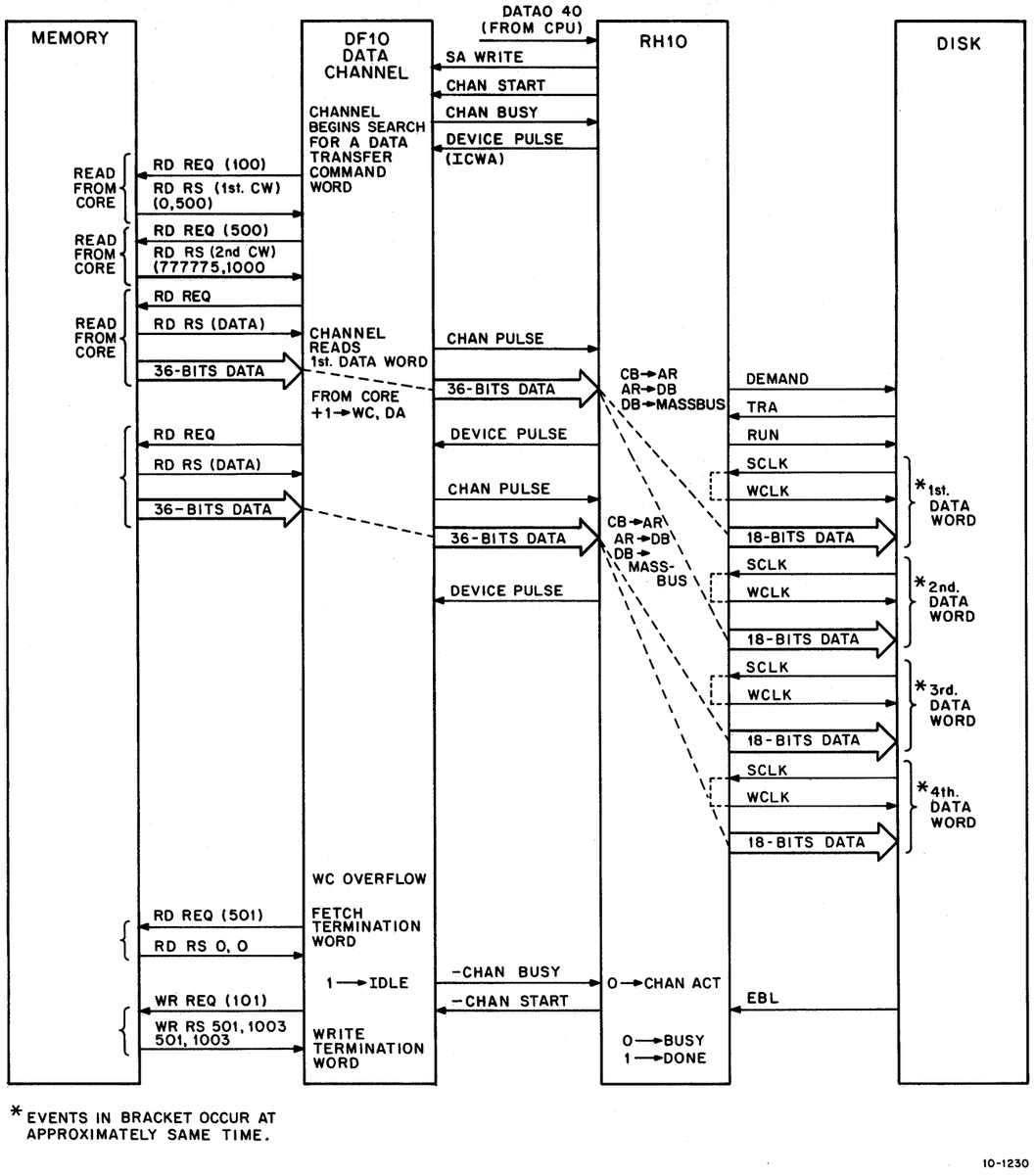


Figure 4-3 Write Data Transfer Interface Diagram

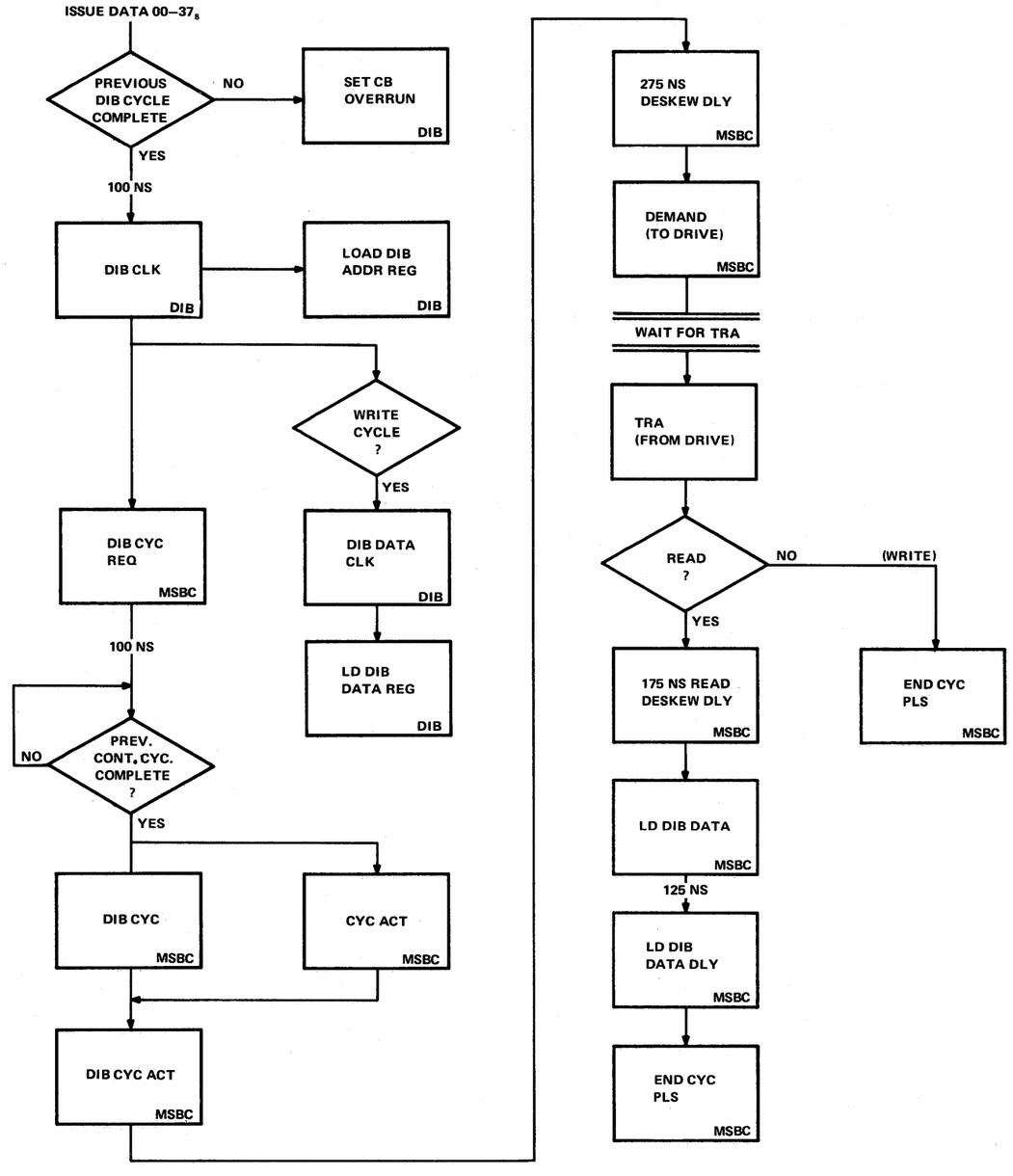


Figure 4-2 DIB Cycle Flow Diagram

placed on the Massbus. On the trailing edge of SCLK, the drive strobes the data into its data buffer. Data words continue to be transferred in this manner until word count overflow is detected by the DF10. When this occurs, the DF10 does a control word read request to fetch the next control word (from location 501 in this case), which may be a jump, a control word to initiate another data transfer, or a termination word (all 0's). If the control word is a termination word, the DF10 writes the termination word into memory into the Initial Control Word Address +1 location (101). The left-half of the termination word contains the address of the termination word (501) and the right-half contains the last data word address (1003).

In addition, the termination word causes IDLE in the DF10 to set, which negates CHN BUSY to the RH10. The negation of CHN BUSY causes CC CHAN ACTIVE in the RH10 to be cleared which negates CHN START OUT. When the End-of-Block (EBL) signal is received from the drive, the BUSY flip-flop is cleared and the DONE flip-flop is set, to terminate the transfer.

4.4 READ DATA TRANSFER INTERFACE DIAGRAM DESCRIPTION

Figure 4-4 is an interface diagram of the read data transfer and shows the main signals between the memory, DF10, RH10 and drive and also shows the sequence in which they occur. Time is shown vertically with Time 0 at the top.

Initially, the starting address is loaded into a register in the drive. The DATAO 40_8 instruction is then issued which causes the CR register in the RH10 to be loaded with the drive select bits, initial control word address, and a read function code with the GO bit set (71_8). The CR register (register 0) is automatically addressed when doing a control cycle so it is not necessary to specify the register. Loading the CR register causes CC ACTIVE BUF in the RH10 to set which, in turn, sets CC CHAN ACTIVE. CC CHAN ACTIVE asserts CHN START OUT to start the DF10 Data Channel. The DF10 receives CHN START OUT and transmits CHN BUSY IN to the RH10 which causes the RH10 to assert CC CHAN SEIZED, indicating that the RH10 has control of the DF10. CC CHAN SEIZED also causes a DEV PLS to be transferred to the DF10 along with the Initial Control Word Address (ICWA). The DF10 strobes the ICWA which is normally a jump instruction to a control word. The diagram shows an Initial Control Word Address of 100. The DF10 fetches the contents of location 100 which contains 0, 500. This instruction dictates that the program jumps to location 500. The DF10 then fetches the contents of location 500 which contains a valid control word of (777775, 1000). This instruction dictates a two-word read operation is to be performed at location 1000 + 1 (1001). Once the valid control word has been fetched by the DF10, it sends a CHAN PLS to the RH10. When the RH10 receives CHAN PLS, it initiates a Massbus control cycle which loads the read function code and GO bit in the Control register of the drive from which the data is to be read. The RH10 issues a DEM to the drive along with the read function code and GO bit. Upon receipt of DEM, the drive issues TRA. The RH10 then issues RUN to the drive and the drive responds with OCC. This initiates the data transfer and connects the drive to the synchronous (data transfer) portion of the Massbus.

The RH10 now waits for Sync Clock (SCLK) signals from the drive. Each 18-bit data word transferred is accompanied by a SCLK signal. The drive presents data on the leading edge of SCLK and the RH10 will strobe the data into its Data Buffer (DB) register on the trailing edge of SCLK. After the data has stabilized in the DB, parity is checked and the data is strobed into the left-half of the Assembly Register (AR). The next 18-bit word, accompanied by the second SCLK, is strobed into the DB, and after it has stabilized, parity is checked and the data is transferred to the right-half of the AR. This fills the 36-bit AR register and sets the AR FULL flip-flop. The 36 bits of data in the AR are then clocked into the Channel Buffer (DB) register. This causes the RH10 to issue a DEV PLS. Both the data word from the CB and the DEV PLS are sent to the DF10 Data Channel.

The DF10, in turn, transfers the data word to memory by issuing a WR REQ. Upon receipt of the data word, the memory returns WRRS, signaling the DF10 that it is ready to accept another word. The DF10, in turn, signifies that it is ready to accept another word from the RH10 by issuing CHAN PLS to the RH10.

To summarize the data transfer, each data word from the drive is sent to the RH10 accompanied by SCLK. The word is transferred successively to the DB, the AR, and the CB. When the word is in the CB, the RH10 issues a DEV PLS, telling the DF10 that it has a word ready for transfer. The DF10 accepts the word and returns a CHAN PLS indicating receipt of the word. The DF10, in turn, transfers the word to core by issuing a WR REQ. When the word is strobed into core, memory issues WRRS, indicating that it is ready to accept another word.

Words continue to be transferred to memory in this manner until word count overflow occurs in the DF10. At this point, the DF10 will initiate a Control Word Read Request

to fetch the next control word (from location 501 in this case) which may be a jump, a control word to initiate another data transfer, or a termination word (all 0's). If the control word is a termination word, the DF10 writes the termination word into memory into the Initial Control Word Address + 1 memory location (101). The left-half of the termination word contains the address of the termination word (501) and the right-half contains the last data word address (1003).

In addition, the termination word causes IDLE in the DF10 to set which negates CHN BUSY to the RH10. The negation of CHN BUSY causes CC CHAN ACTIVE in the RH10 to be cleared which negates CHN START OUT. When the End-of-Block (EBL) signal is received from the drive, the BUSY flip-flop is cleared and the DONE flip-flop is set to terminate the transfer.

4.5 WRITE DATA TRANSFER FLOW DIAGRAM

The write data transfer is initiated by the DATAO 40_8 instruction which is placed on the I/O bus. If the RH10 is busy, the instruction is ignored. If the RH10 is not busy, the CR register is loaded with the Initial Control Word Address (ICWA), the write function code and the GO bit (Figure 4-5a). The write function code is 61_8. In addition, the CR register is loaded with DR SEL (drive select) bits specifying one of the drives in the system.

Prevent Start (PREV START) conditions will cause the RH10 to terminate. These PREV START conditions are Power Supply Fail (PS FAIL), Illegal Function Code (ILFC) or a Register Access Error in the Selected Drive (RAE SEL DR). If any of these conditions occur, the corresponding error bit is set to terminate the transfer.

With none of the above conditions present, the BUSY flip-flop in the RH10 is set. The RH10 issues a CHAN START signal to the DF10 Data Channel. If the DF10 is busy, the RH10 waits until it becomes free. When this occurs, the DF10 transmits a CHN BUSY IN signal to the RH10. The RH10 now assumes control of the data channel, puts the ICWA on the channel bus and issues a Device Pulse (DEV PLS).

The DF10 fetches the first control word from memory. This word is stored in the Initial Control Word Address location, and usually consists of a jump to another Control Word Address. The second control word is then fetched and normally contains the Word Count (WC) in the left-half, and Data Address (DA) in the right-half. The WC and DA are stored in their respective DF10 registers. The WC register specifies the number of data words to be transferred and the DA specifies the first core memory location to be read from. The first data word is transferred to the RH10 along with a Channel Pulse (CHN PLS). The word is loaded in the CB register. The DF10 then fetches the next data word from memory.

Each data word is transferred to the RH10 starting at the DA + 1 location. The WC register is decremented (WC is loaded with 2's complement and is incremented) for each data word and the DA is incremented for each data word. When the WC overflows, the number of words initially specified have been transferred and the next control word is fetched from core memory. If the control word contains all 0's, the end of communications is specified and the data channel terminates operation.

At this point, the flow diagram divides into two paths – one path initiating the Massbus control bus cycle and the second path designated DF10 WRITE LOOP which is shown in Figure 4-5b. The Massbus control bus cycle is described first and is followed by a description of the DF10 WRITE LOOP (Paragraph 4.5.2).

4.5.1 Massbus Control Bus Cycle

A control cycle is initiated on the Massbus as a result of CHN PLS from the DF10. This indicates that the DF10 is ready to receive data or has transmitted the first data word. The control cycle causes the information stored in the CR register in the RH10 to be transferred to the Massbus. This information includes the function code (61_8 for a write), and the selected drive. The RH10 issues a DEM signal to the drive. When the selected drive accepts the function code and GO bit, it returns TRA indicating receipt of the data.

NOTE

If the drive does not respond to DEM within 1.5 μs or a non-existent drive has been addressed, a Control Bus Timeout (CBTO) occurs and causes CR Drive Response Error (CR DR RESP ERR) to set. This causes the BUSY flip-flop to clear, the DONE flip-flop to set, and the data transfer to terminate.

The RH10 initiates the Massbus data bus cycle (where the data transfer will occur) by issuing a RUN signal. The drive issues OCC to the RH10 indicating receipt of RUN.

NOTE

If the drive does not respond to RUN within 10 ms, a Data Bus Timeout (DBTO) occurs and causes CR DR RESP ERR to set. This causes the BUSY flip-flop to clear, the DONE flip-flop to set and the data transfer to terminate.

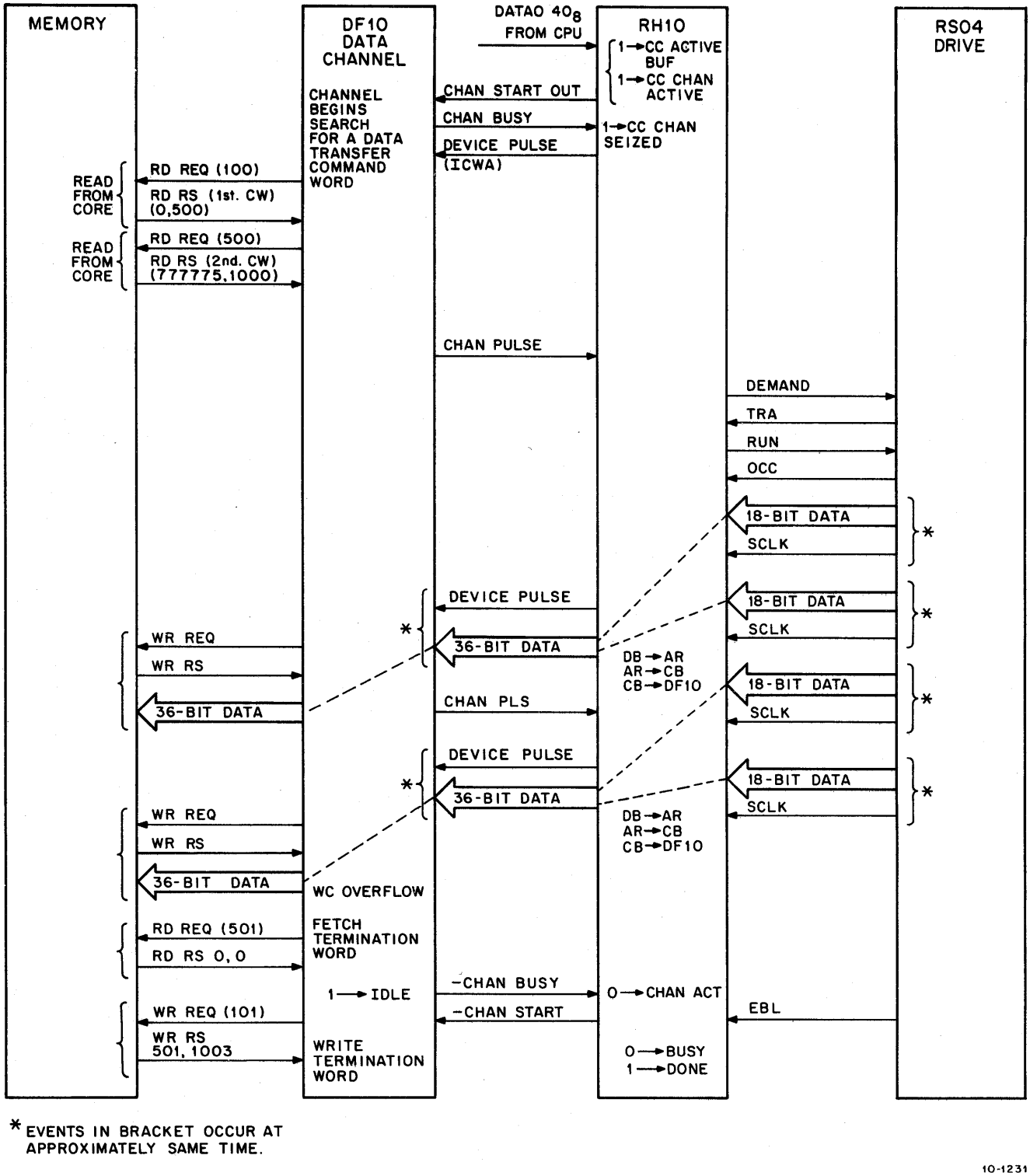


Figure 4-4 Read Data Transfer Interface Diagram

At this point, the flow again divides into two paths – an error termination path and a RH10 WRITE LOOP. The error termination path is described first. The RH10 WRITE LOOP is described in Paragraph 4.5.2.

If there are no error conditions, the flow on Figure 4-5a is completed. However, if DXES is set (Disable Transfer Error Stop), the transfer will continue until normal termination for Class A errors (non-catastrophic). For Class B (catastrophic) errors, the drive will terminate immediately, resulting in the setting of CR CBTO which causes CXR BUSY to clear and CXR DONE to set.

4.5.2 DF10 and RH10 WRITE LOOP

The DF10 and RH10 WRITE LOOPs are interrelated and both are consequently described in this paragraph.

The CHN PLS accompanies the data word from the DF10. The word is temporarily stored in the CB. If there is a Channel Bus Data Parity Error (CDPE) and CR DXES is set, the CDPE is set, the CHAN START signal is negated and the data transfer is terminated. If DXES is reset, normal operation is continued.

If the AR is empty, the data word from the CB is loaded into the AR and the RH10 immediately requests another word from the CB since the CB is now empty. The RH10 requests a new data word by issuing DEV PLS. When the DF10 is ready to send a new word, it issues CHN PLS and transfers the word to the CB.

Meanwhile, the first data word which is stored in the AR is transferred to the DB.

NOTE

The CB and AR are 36-bit registers and the DB is an 18-bit register. It therefore takes two cycles to transfer a 36-bit word from the AR to the drive via the DB.

The Massbus control bus cycle (DEM-TRA) and Massbus data bus cycle (RUN-OCC) have been initiated at this point and the drive issues a Sync Clock (SCLK) signal indicating it is prepared to accept the first data word. The RH10 receives the SCLK and reroutes it back to the drive as a WCLK. The drive will strobe the data off the bus on the leading edge of WCLK and the RH10 will load the second byte into the DB register on the trailing edge of SCLK. Since the AR is now empty, it immediately obtains a new data word from the CB which, in turn, received the word from the DF10.

NOTE

If a SCLK is transmitted by the drive while the AR is empty and the DF10 is still active, an overrun condition exists, the OVERRUN error is set, the CHN START signal is dropped, and the data transfer is terminated. If the SCLK is received while the AR is empty and the DF10 Data Channel is inactive, 0's are loaded into the DB and onto the Massbus, causing the remainder of the sector to be zero-filled.

The process of transferring words from the memory to the drive continues until the end of the sector is reached. When this occurs, the drive issues an End-of-Block (EBL) signal to the RH10. If the RUN line is still asserted on the Massbus, data transfer of the next sector is initiated. If the RUN line is negated, the data transfer is terminated.

If a drive error occurs, the Exception (EXC) line is raised and causes DR EXC to be set. If the error is a Class B error, the BUSY flip-flop is cleared, the DONE flip-flop is set and the transfer is immediately terminated. If the error is a Class A error, the channel is first terminated, the BUSY flip-flop is cleared, the DONE flip-flop is set and the data transfer is terminated. If the first channel pulse has not been received, the channel is not active and consequently cannot be terminated. In this case, the data transfer is immediately terminated.

4.6 READ DATA TRANSFER FLOW DIAGRAM DESCRIPTION

The read data transfer is initiated by the DATAO 40_8 instruction which is placed on the I/O bus. If the RH10 is busy, the instruction is ignored. If the RH10 is not busy, the CR register is loaded with the Initial Control Word Address (ICWA), the read function code and the GO bit (Figure 4-5a). The read function code is 71_8. In addition, the CR register is loaded with the Drive Select (DR SEL) bits, specifying one of the drives in the system.

A PREV START condition will cause the RH10 to terminate. These PREV START conditions are Power Supply Fail (PS FAIL), illegal function code, or a Register Access Error in the Selected Drive (RAE SEL DR). If any of these conditions occur, the corresponding error bit is set to terminate the transfer.

With none of the above conditions present, the BUSY flip-flop in the RH10 is set. The RH10 issues a CHAN START signal to the DF10 Data Channel. If the DF10 is busy, the RH10 waits until it becomes free. When this

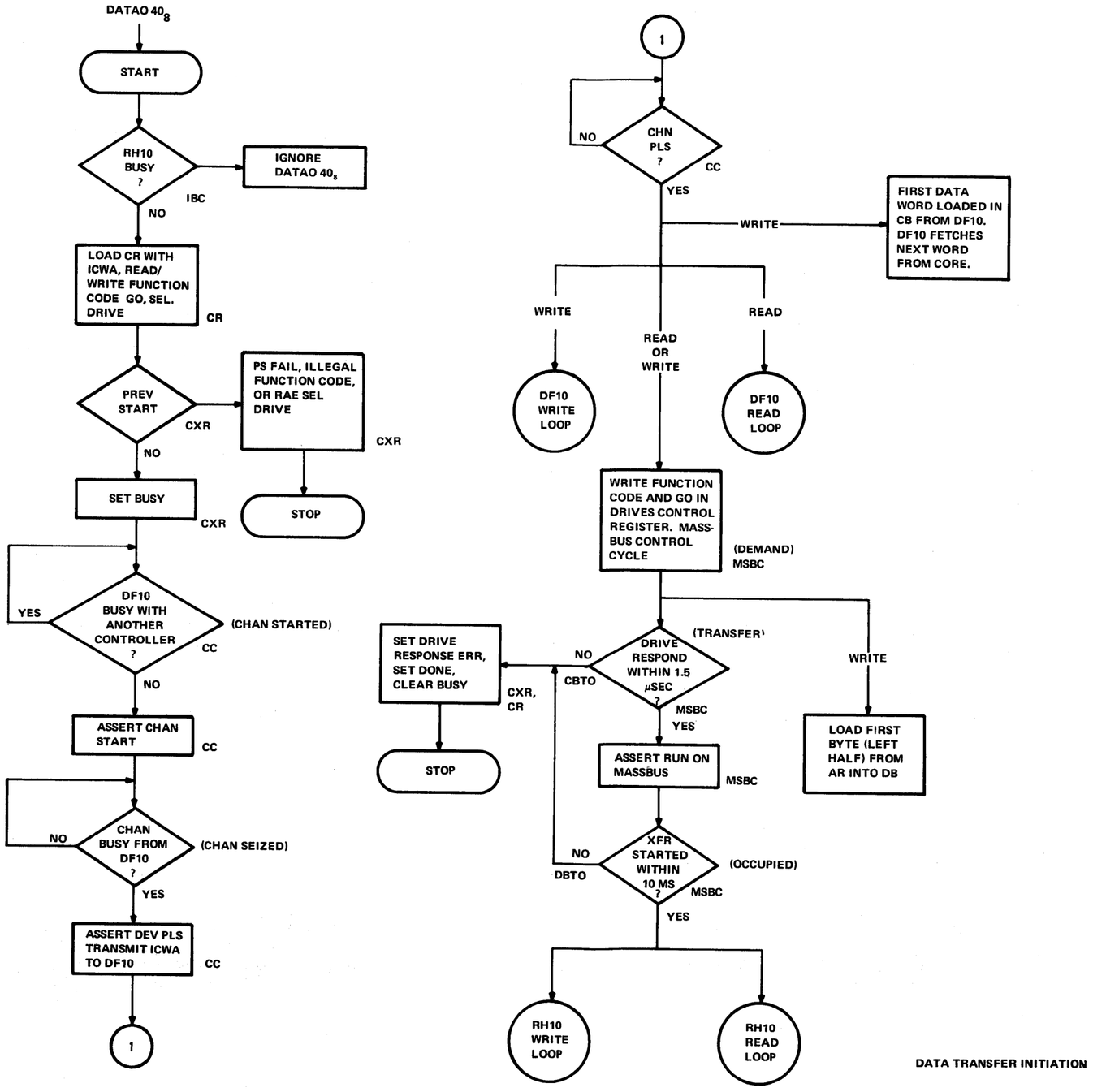


Figure 4-5a Read/Write Data Transfer Detailed Flow Diagram

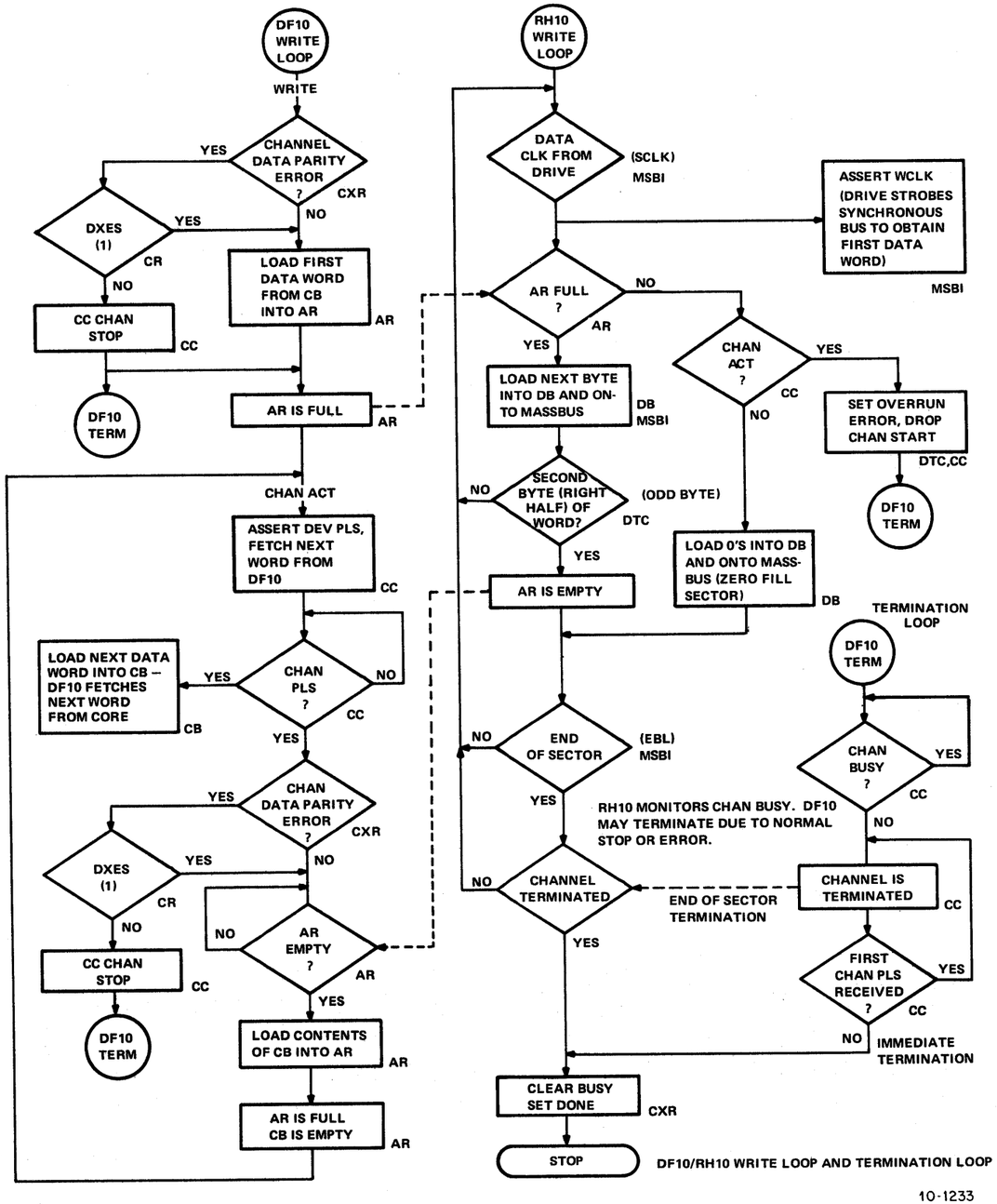


Figure 4-5b Read/Write Data Transfer Detailed Flow Diagram

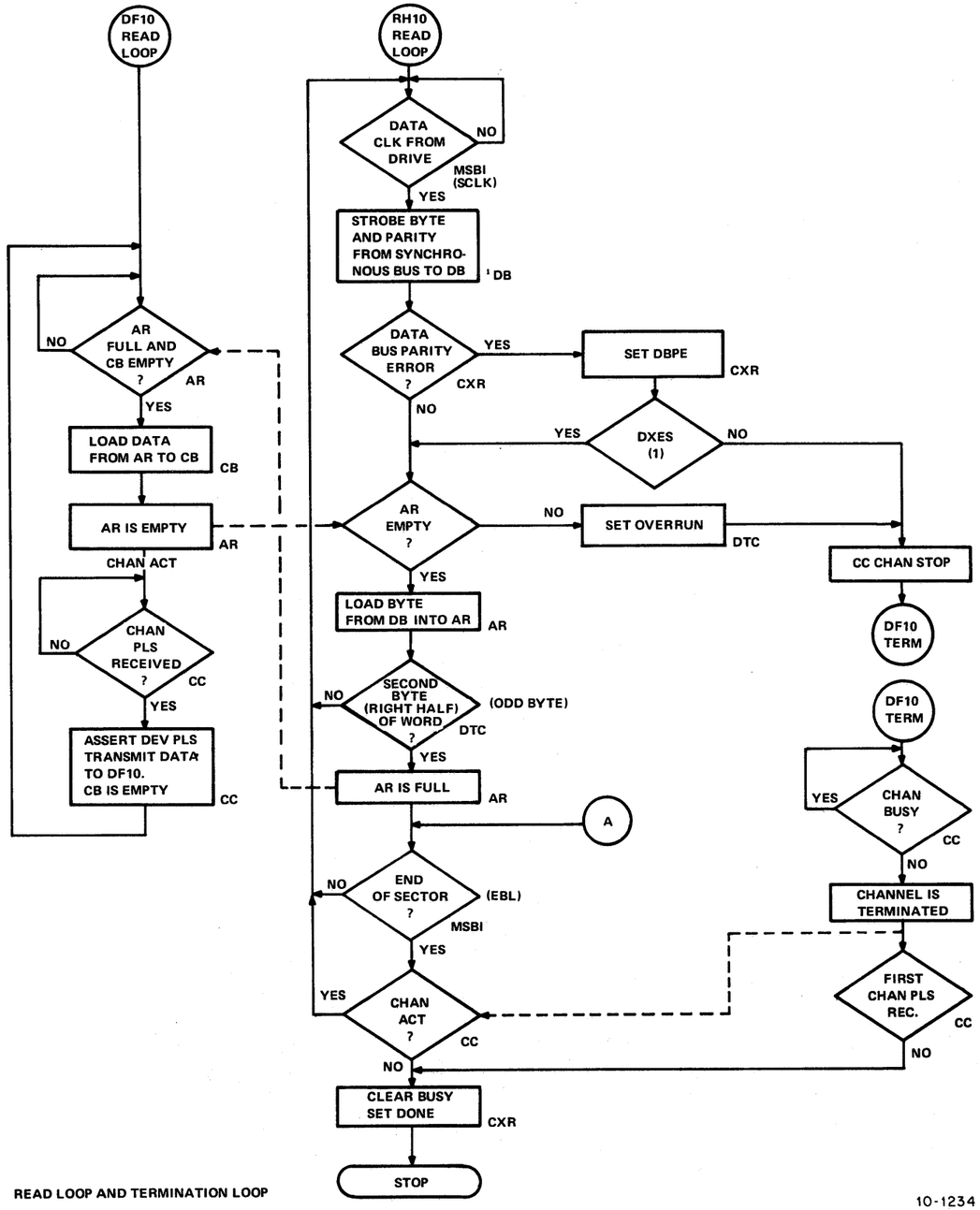


Figure 4-5c Read/Write Data Transfer Detailed Flow Diagram

occurs, the DF10 transmits a CHN BUSY IN signal to the RH10. The RH10 now assumes control of the data channel, puts the ICWA on the channel bus and issues a Device Pulse (DEV PLS). When the DF10 accepts the initial control word address, it issues a Channel Pulse (CHN PLS) back to the RH10.

The DF10 fetches the first control word from memory. This word is stored in the Initial Control Word Address location, and usually consists of a jump to another control word address.

The second control word is then fetched and normally contains the Word Count (WC) in the left-half, and Data Address (DA) in the right-half. The WC and DA are stored in their respective DF10 registers. The WC register specifies the number of data words to be transferred and the DA specifies the first core memory location to be read.

Each data word from the drive is transferred to the DF10, accompanied by a DEV PLS. Each word is then transferred to core memory starting at the DA location. The WC register is decremented (WC is loaded with 2's complement and is incremented) for each data word while the DA is incremented for each data word. When the WC overflows, the number of words initially specified have been transferred and the next control word is fetched from core memory. If the control word contains all 0's, the end of communication is specified and the data channel terminates operation.

At this point, the flow diagram divides into two paths – one path initiating the Massbus control bus cycle and the second path designated DF10 READ LOOP which is shown in Figure 4-5c. The Massbus control bus cycle is described first and is followed by a description of the DF10 READ LOOP (Paragraph 4.6.2).

4.6.1 Massbus Control Bus Cycle

A control cycle is initiated on the Massbus as a result of CHN PLS from the DF10 and causes the information stored in the RH10 Control register to be transferred to the Massbus. This information includes the function code (71_8 for a read), and the selected drive. The RH10 issues a DEM signal to the drive. When the selected drive accepts the function code and GO bit, it returns TRA indicating receipt of the data.

NOTE

If the drive does not respond to DEM within 1.5 μs or a non-existent drive has been addressed, a Control Bus Timeout (CBTO) occurs and causes CR Drive Response Error (CR DR RESP ERR) to set. This causes the BUSY flip-flop to clear, the DONE flip-flop to set, and the data transfer to terminate.

The RH10 initiates the Massbus data bus cycle by issuing a RUN signal. The actual data transfer occurs on the data bus. The drive issues OCC to the RH10 indicating receipt of RUN.

NOTE

If the drive does not respond to RUN within 10 ms, a Data Bus Timeout (DBTO) occurs and causes CR DR RESP ERR to set. This causes the BUSY flip-flop to clear, the DONE flip-flop to set and the data transfer to terminate.

At this point, the flow again divides into two paths – an error termination path and a RH10 READ LOOP. The error termination path is described first. The RH10 READ LOOP path is described in Paragraph 4.6.2 in conjunction with the DF10 READ LOOP path. However, if Disable Transfer Error Stop (DXES) is set, then the transfer will continue until normal termination for Class A errors (non-catastrophic). For Class B (catastrophic errors), the drive will terminate immediately resulting in the setting of CR CBTO which causes CXR BUSY to clear and CXR DONE to set.

4.6.2 DF10 and RH10 READ LOOP

The DF10 and RH10 READ LOOPs are interrelated; consequently, both are described in this paragraph. The RH10 READ LOOP basically loads data from the drive into the AR via the DB register. The DF10 READ LOOP basically loads data into the DF10 from the AR via the CB register.

After the Massbus control bus (DEM-TRA) and data bus (RUN-OCC) cycles have been initiated, the drive puts data words on the Massbus accompanied by Sync Clock (SCLK) signals. The data is strobed into the DB register in the RH10. If there is a Data Bus Parity Error (DBPE), and

DXES is reset, the DBPE error is set, the CHAN START signal is dropped and the data transfer is terminated. If DXES is set, normal operation is continued. If a SCLK is received while the AR is full, the drive is sending words faster than the DF10 is accepting them; consequently, the OVERRUN error bit is set, the CHAN START signal is dropped, and the data transfer is terminated.

Under normal operation, the AR is empty while the DB is loaded from the Massbus. Consequently, the data word from the DB is loaded into the left-half of the AR. It should be remembered that the DB is an 18-bit register and the AR and CB are 36-bit registers. The ODD BYTE flip-flop is toggled to the set state. The state of this flip-flop designates which byte is in the DB register. The next SCLK from the drive accompanies the second data word which is clocked into the DB. The ODD BYTE flip-flop is again toggled. At this point, the AR is full and the word is strobed into the CB as soon as the CB is empty. An AR FULL flip-flop and CB FULL flip-flop designate the state of the AR and CB register, respectively. When the word is transferred to the CB, (a) the data word in the CB is transferred to the DF10 Data Channel accompanied by a DEV PLS, and (b) the AR is now empty to accept another data word from the DB. Thus, the data words flow from the drive to the DB, to the AR, to the CB, and finally to the DF10 Data Channel and core memory.

The process of transferring the data words continues until the end of a sector is reached. At this point, the drive issues an End-of-Block (EBL) signal. If the RUN signal is still asserted, a data transfer for the next sector is initiated. If the RUN signal is negated, the data transfer is terminated to complate the operation. However, if a drive error occurs, the Exception (EXC) line is raised and causes DR EXC to be set. If the error is a Class B error, the BUSY flip-flop is cleared, the DONE flip-flop is set and the transfer is immediately terminated. If the error is a Class A error, the channel is first terminated, the BUSY flip-flop is cleared, the DONE flip-flop is set and the data transfer is terminated. If the first channel pulse has not been received, the channel is not active and consequently cannot be terminated. In this case, the data transfer is immediately terminated.

4.7 KA10 AND KI10 INTERRUPTS

The RH10 contains interrupt logic to interrupt the KA10 processor with a priority level interrupt or to interrupt the KI10 processor with a priority level interrupt or a vector interrupt. KA10 or KI10 interrupt is selected by the IADR KI10 INTR flip-flop (see RH10-0-IADR). When set, the flip-flop denotes a KI10 interrupt and, when reset, denotes a KA10 interrupt.

In the KA10, the Priority Interrupt (PI) channel is set in the RH10 via a CONO instruction from the KA10. When an error or done condition occurs in the RH10, the RH10 raises the appropriate PI level, which causes the KA10 to interrupt to a subroutine entry address equal to 40 plus 2 times the channel number. For example, if the RH10 interrupts the KA10 on PI channel 7, the processor interrupts to 54.

The KI10 priority level interrupt works in a similar fashion to the KA10 interrupt. However, the KI10 can interrupt to a vector address in addition to a priority level interrupt. The basic process of interrupting to a vector address is initiated by a CONO instruction which sets up the PI channel in the RH10. A DATAO instruction is then issued to the RH10 to load the vector address into the Interrupt Address register, and to select the KA or KI10 interrupt.

NOTE

In a KA10 interrupt, it is not necessary to perform the DATAO; the IADR KI10 INTR flip-flop is reset indicating a KA10 interrupt.

When the error or done condition raises the interrupt, it is sent to the KI10, which recognizes the PI level and returns IOB PI REQ SYNC, together with the channel number of the request it is to honor. This is sent via IOB bits 00–02. The RH10 compares the channel number just received from the KI10 with the channel number previously sent. If the two compare, this indicates that the RH10 was the device which caused the interrupt. The KI10 will then generate IOB PI GRANT which, in turn, asserts IADR PI START in the RH10. The vector address is put on the I/O bus to be collected by a DATAI. Also if the KI10 is to perform a vector interrupt, a function code of 2 is established by the RH10 and is returned to the KI10 via bits 4 and 5 of the I/O bus. When doing a KI10 vector interrupt, the vector address from the IADR register is sent to the KI10 in addition to the function code. The KI10 now does a vector interrupt as specified by the function code and traps to the vector address specified in the IADR register.

4.8 READ-IN MODE

The Maintenance Switch Panel (Figure 6-3) contains a read-in feature to allow Massbus devices to be boot-strapped. As a result, the program in the Massbus device is to be transferred to core where it is under control of the CPU. A thumbwheel switch on the switch panel allows the operator to select the drive on the "daisy-chain" which is to be read. When the read-in is initiated at the CPU console, a READ command is generated by the hardware for this device. For bootstrapping disks, the starting address is

always the least significant address for that device; i.e., track 0 sector 0 for a fixed-head disk. For bootstrapping magnetic tapes, a REWIND command is generated by the hardware prior to the read.

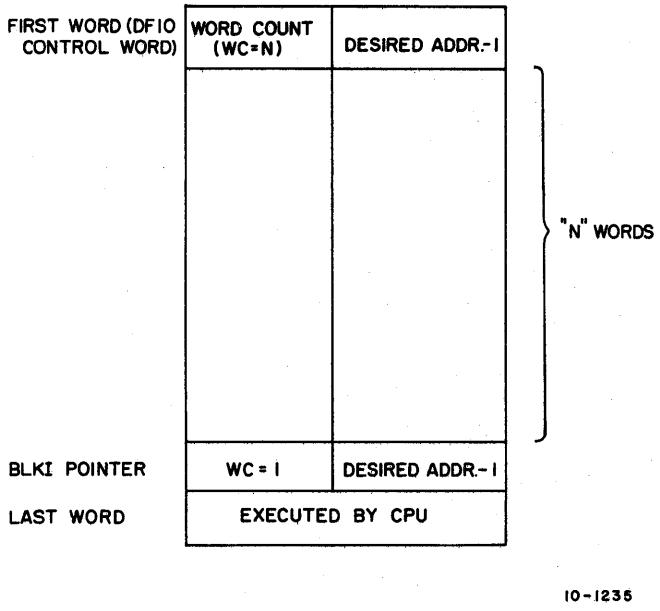


Figure 4-6 Bootstrap Data Block

The data transfer initiated by read-in mode occurs via the DF10 Data Channel with the exception of the last 2 words in the bootstrap data block. In order to accomplish this, the first word in the data block must be treated as a control word and not a data word. The format of the bootstrap data block is shown in Figure 4-6. Note that the first word is a control word with the left-half comprising the word count and the starting core address, minus one, in the right-half. The word count should be such that the last and the next to last words in the bootstrap data block are not transferred to core. These two words are handled by the hardware as follows.

After transferring n words, the DF10 terminates, IOB RDI DATA is asserted by the RH10, and the CPU will fetch the next to last word in the data block via the I/O bus. This word is the pointer for the BLKI and should contain a word count of 1 in the left-half. The BLKI is automatically generated by the CPU for a read-in operation. The CPU will then read and execute the last word in the data block via the I/O bus with the BLKI to terminate the read-in.

CHAPTER 5
DETAILED LOGIC DESCRIPTION

5.1 GENERAL

This chapter provides a detailed logic description of drive register read and write operations, read and write data transfers, priority and vector interrupt logic and read-in mode.

5.2 DIB CYCLE

A DIB cycle is performed in order to read or write a drive register. The DIB cycle for a drive register write operation transfers the data from the I/O Bus to the Drive Interface Buffer (DIB) in the RH10. A Massbus cycle is then initiated to transfer the data from the DIB to the desired drive register. The DIB cycle for a drive register read operation initiates a Massbus cycle to transfer the data from the drive register to the DIB in the RH10. In order to read the register, the programmer would issue a DATAI which would gate the contents of the DIB register onto the I/O Bus.

Paragraph 5.2.1 contains a detailed description of the DIB write cycle and Paragraph 5.2.2 contains a detailed description of the DIB read cycle.

5.2.1 DIB Write Cycle Detailed Description (Figure 5-1)

The DIB write cycle is initiated by a DATAO to the RH10 DIB register (address $00–37_8$, Figure 3-11). The RH10 is selected as a result of 270_8 being decoded from the I/O bus device select lines (IBC IOB IOS3 – IBC IOB IOS9). If there is no overrun condition, IBC DATAO CLR is asserted.

NOTE

The overrun condition occurs if a DATAO is issued before the previous DIB cycle has completed.

IBC DATAO CLR generates DIB CLK after a 100-ns delay if the following conditions are true:

1. IOB 00 is negated indicating a DIB cycle
2. There is no register access error (~RAE) or the CXR RAE EN flip-flop is reset [CXR RAE EN (0)] if there is a register access error
3. A previous overrun condition has not been detected [CB OVERRUN (0)].

The DIB CLK, when asserted, clocks the address information from the I/O bus into the DIB register which interfaces to the Massbus. This information consists of the drive register selected (bits 00–05), a write operation (LR bit 06 = 1), and the drive selected (bits 15–17). The DIB CLK generates DIB DATA CLK during a DIB write cycle since LR bit 06 = 1. The DIB DATA CLK clocks the data from the I/O bus into the data portion of the DIB register (bits 20–35), if no cycle is in progress. DIB CLK also initiates a Massbus control bus cycle to cause the data in the DIB register to be written into the drive, by setting MSBC DIB CYC REQ which does the following:

1. DIB CYC REQ generates MSBC REQ PLS. This asserts MSBC DIB CYC, indicating a DIB CYCLE is requested.
2. 100 ns after MSBC DIB CYC REQ, MSBC CYC ACT is set, indicating a Massbus DIB cycle is in progress.

NOTE

If a previous cycle is in progress, MSBC CYC ACT (1) inhibits MSBC REQ PLS which inhibits the DIB CYC flip-flop from setting.

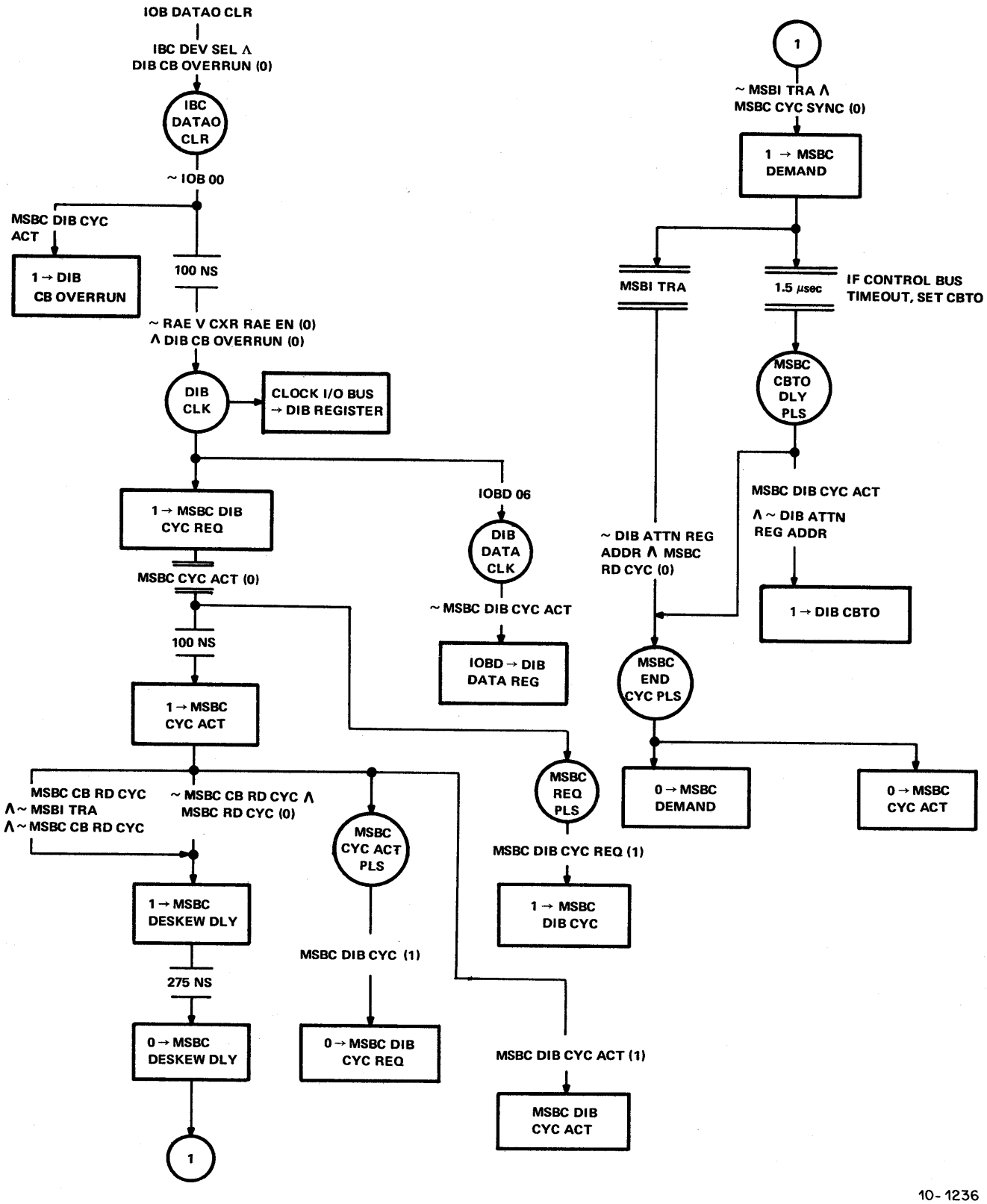


Figure 5-1 DIB Write Cycle Flow Diagram

MSBC CYC ACT generates MSBC CYC ACT PLS which is used to clear MSBC DIB CYC REQ. MSBC CYC ACT also initiates the 275-ns deskew delay (MSBC DESKEW DLY) to allow the address and data lines at the output of the DIB register time to stabilize at the drive end. ~MSBC CB RD CYC and MSBC RD CYC 0 denotes a DIB write cycle and also denotes the previous cycle was a write cycle. If the previous cycle was a read [MSBC RD CYC (1)], then MSBC DESKEW DLY cannot be asserted until MSBI TRA is negated.

The RH10 then issues DEM, if MSBC CYC SYNC is reset and TRA is not present from a previous Massbus control bus cycle. The drive, upon receipt of DEM, strobes the data from the Massbus into its data buffer and issues TRA.

NOTE

If the RH10 does not receive TRA from the drive within 1.5 μs, a control bus timeout occurs. CBTO DLY PLS is generated which clocks the DIB CBTO flip-flop set. This is reflected in bit 7 of the DIB register.

Since MSBC RD CYC is reset and the Attention Summary is not being addressed, MSBC END CYC PLS is generated upon receipt of MSBI TRA. This clears the DEM and CYC ACT flip-flops to terminate the cycle. If a control bus timeout occurred due to the RH10 not receiving TRA within 1.5 μs of DEM, CBTO DLY PLS would generate END CYC PLS to clear the DEM and CYC ACT flip-flops.

5.2.2 DIB Read Cycle Detailed Description (Figure 5-2)

The DIB read cycle is initiated by a DATAO to the DIB register (address $00–37_8$, Figure 3-11). The RH10 is selected as a result of 270_8 being decoded from the I/O bus device select lines (IBC IOB IOS 3 – IBC IOB IOS 9). If there is no overrun condition, IBC DATAO CLR is asserted.

NOTE

The overrun condition occurs if a DATAO is issued before the previous DIB cycle has completed.

IBC DATAO CLR generates DIB CLK after a 100-ns delay if the following conditions are true:

1. IOB 00 is negated indicating a DIB cycle (~IOB 00),
2. There is no register access error, (~RAE), or the CXR RAE EN flip-flop is reset if there is a register access error
3. A previous overrun condition has not been detected [CB OVERRUN (0)].

The DIB CLK, when asserted, clocks the address information from the I/O bus into the DIB register which interfaces to the Massbus. This information consists of the drive register selected (bits 00–05), a read operation (LR bit 06 = 0), and the drive selected (bits 15–17). The DIB CLK generates MSBC DIB CYC REQ to initiate a Massbus control bus cycle to transfer the address information to the drive.

MSBC DIB CYC REQ generates MSBC REQ PLS and also generates MSBC CYC ACT after a 100-ns delay. MSBC REQ PLS and MSBC DIB CYC REQ (1) cause MSBC DIB CYC to set which, in turn, asserts MSBC DIB CYC ACT indicating a DIB cycle is in progress.

MSBC CYC ACT PLS is generated as a result of MSBC CYC ACT and causes the MSBC DIB CYC REQ flip-flop to reset. MSBC CYC ACT also initiates the 275-ns deskew delay (MSBC DESKEW DLY) to allow the address lines at the output of the DIB register time to stabilize at the drive end. At the end of the 275-ns deskew delay, the RH10 asserts DEM on the Massbus if MSBC CYC SYNC is reset and there is no TRA signal from a previous Massbus control bus cycle. The drive strobes the Massbus lines and ascertains the desired register to be read. The contents of the register and TRA are placed on the Massbus.

NOTE

If the drive does not respond to DEM within 1.5 μs, a control bus timeout occurs. CBTO DLY PLS is generated which clocks the DIB CBTO flip-flop set. This is reflected in bit 7 of the DIB register.

175 ns after TRA is received from the drive, MSBC LD DIB DATA is generated. This delay allows a deskew of the data on the Massbus before it is strobed into the DIB register.

Since the Attention Summary register is not being addressed and since MSBC RD CYC is set, the LD DIB DATA signal is generated. The LD DIB DATA signal creates DIB DATA CLK which clocks the data from the Massbus into the DIB register. If the parity bit from the drive is asserted, it is loaded into the PAR CPA flip-flop at the time of DIB DATA CLK reflecting the status of the parity bit in the drive.

When the data has been loaded into the DIB register, parity is computed and 125 ns after MSBC LD DIB DATA is generated, MSBC LD DIB DATA DLY is generated. This signal performs two functions. It clocks the Control Bus Parity Error (CBPE) flip-flop and if the parity is even, CBPE is clocked set. A second function of MSBC LD DIB DATA DLY is to generate END CYC PLS which clears the DEM and CYC ACT flip-flops to terminate the cycle. If a control bus timeout occurred due to the RH10 not receiving TRA within 1.5 μs of DEM, CBTO DLY PLS would generate END CYC PLS to clear the DEM and CYC ACT flip-flops.

5.3 WRITE DATA TRANSFER DETAILED DESCRIPTION

The following paragraphs describe a write data transfer operation in detail. The paragraphs are listed in the same order that the sequence of events occur.

5.3.1 Device Selection

The write data transfer is initiated by a DATAO 40_8 instruction which is placed on the I/O bus by the CPU (Figure 5-3). IOS lines 3–9 on the I/O bus specify the RH10 whose address is decoded as 270_8 as shown below.

IOS3	IOS4	IOS5	IOS6	IOS7	IOS8	IOS9
0	1	0	1	1	1	0
						1
	2			7		0

The RH10 logic contains a jumper card in the event that a system has two RH10's (see RH10-0-IBC, sheet 1). In this case, the first RH10 has the address of 270_8 assigned by the jumper card. The second RH10 has its jumper card assigned for 274_8 which is simply accomplished by changing IOS 9 from a logic 0 to a logic 1. When the CPU places the 270_8 address on the IOS lines, an IBC DEV SEL pulse is generated if the RH10 is not in local mode.

5.3.2 Control Register Selection

When the CPU issues the DATAO 40_8 instruction, the Controller Register Select (CR REG SEL) flip-flops are loaded (see RH10-0-IBC). IOBD 00 is a logic 1 and IOBD 01, 02, and 03 are logic 0's. This loads a 40_8 in the CR REG SEL flip-flops. The output of these flip-flops is decoded by the M152 decoder as IBC CONT REG SEL. This signal is used to generate CR CLOCK which loads one of the RH10 controller registers.

5.3.3 Drive Selection

When the CPU issues the DATAO 40_8 instruction, the selected drive number is loaded via bits 15–17 of the I/O Bus. The CR Clock signal strobes the drive select bits (IOBD15 – IOBD17) into DR SEL flip-flops 00 – DR SEL 02 (see RH10-0-CR). This action selects one of eight drives which may be incorporated in the system.

5.3.4 CR CLOCK

The CR CLOCK pulse is used to clock various flip-flops in the CR register. For a write data transfer, a function code of 61_8 will be loaded, and DTC XFR COMP, IBC CONT REG SEL, and IBC DATAO SET are asserted to generate CR CLOCK A and CR CLOCK B (dual-outputs used for loading purposes). Note that IBC CONT REG SEL was asserted when the CR REG SEL flip-flops were loaded and decoded as 40_8. The CR CLOCK is also used to generate IBC INITIAL CLR which is used to initialize the RH10. In addition, it performs the following functions:

a. Clocks the Initial Address (INAD) from the I/O bus to the INAD register (see RH10-0-CR). This address is contained in bits 21–28 of the I/O bus and is loaded in bits 27–34, respectively, of the INAD register. The INAD address is the starting memory location which contains the first control word.

b. Clocks the function code from bits 30–34 of the I/O bus into the FUNCT CODE register (see RH10-0-CR). The function code specified for a write operation is 61_8.

c. Clocks bit 35 from the I/O bus into the GO flip-flop. The GO flip-flop must be set in order for a data transfer to occur.

5.3.5 Start of Transfer

The trailing edge of CR CLK is applied to a pulse amplifier which generates CR START XFR A and START XFR B pulses (two versions for loading purposes) if the GO bit is set. START XFR B sets the CXR BUSY flip-flop if CXR PREV START is not asserted. If this signal is asserted, the CXR DONE flip-flop is set and the CXR BUSY flip-flop is reset preventing the RH10 from starting a data transfer.

CR START XFR A clocks the CC ACTIVE BUF flip-flop set if CC CHAN START EN is asserted. This signal is asserted if the RH10 is not in local mode or if the RH10 is in local mode with the switch panel CHAN EN switch on.

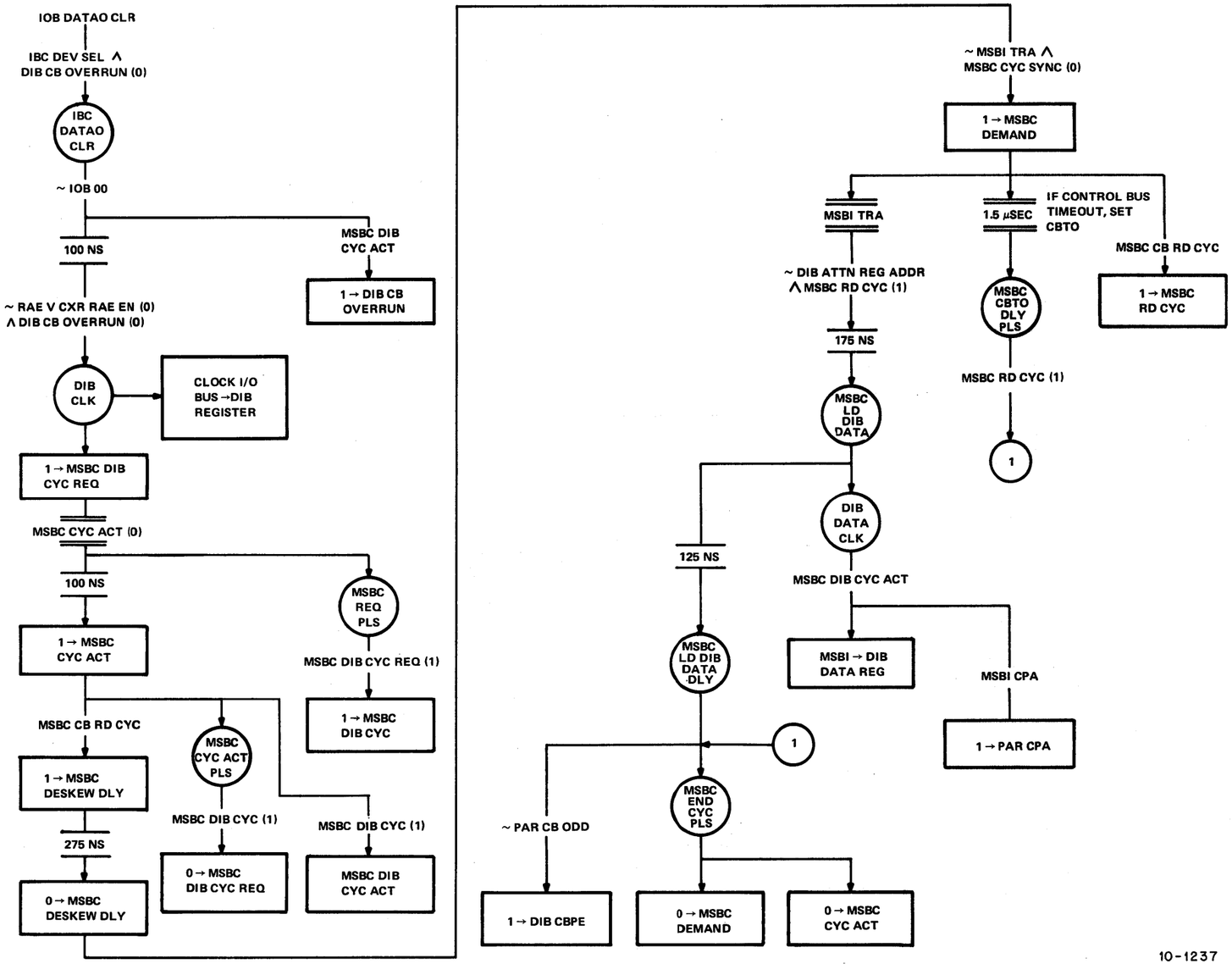
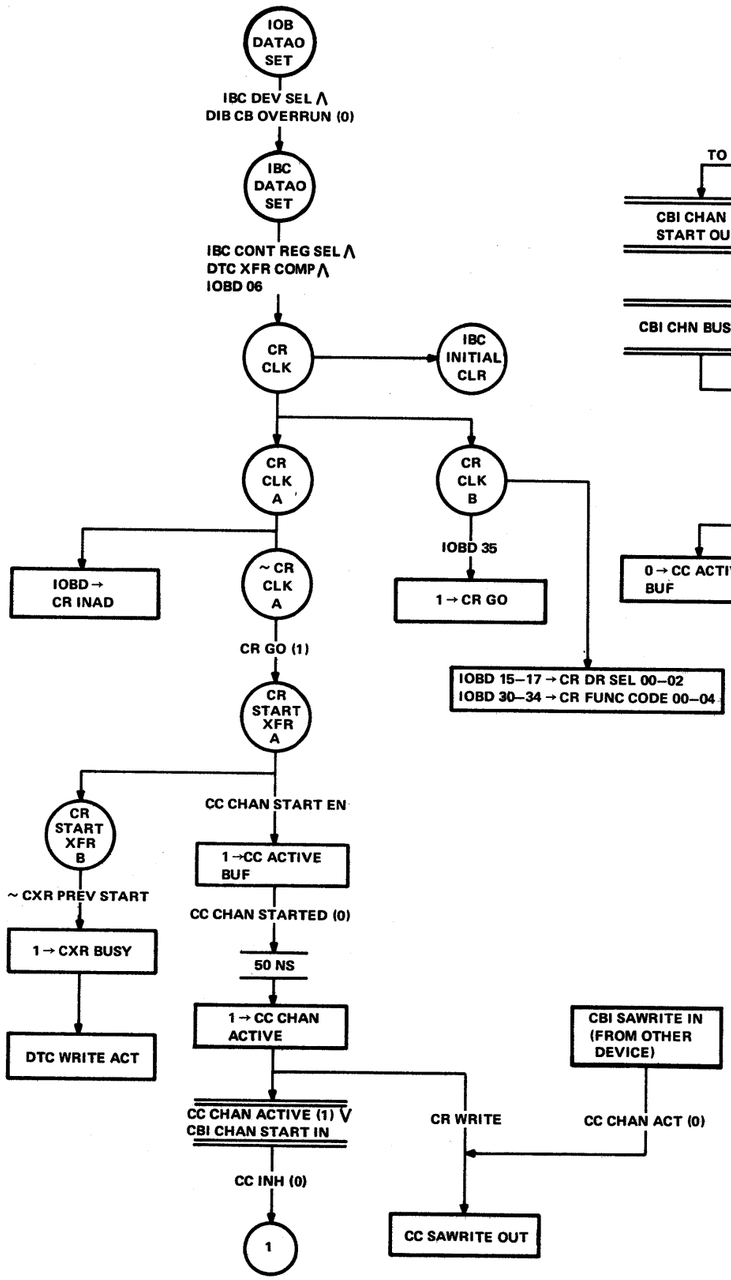
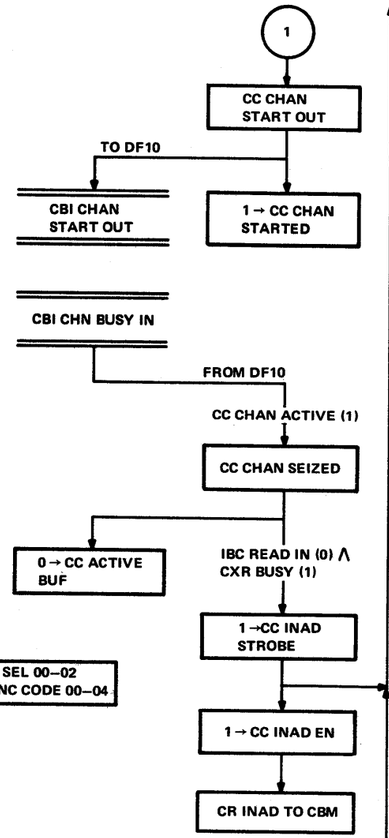
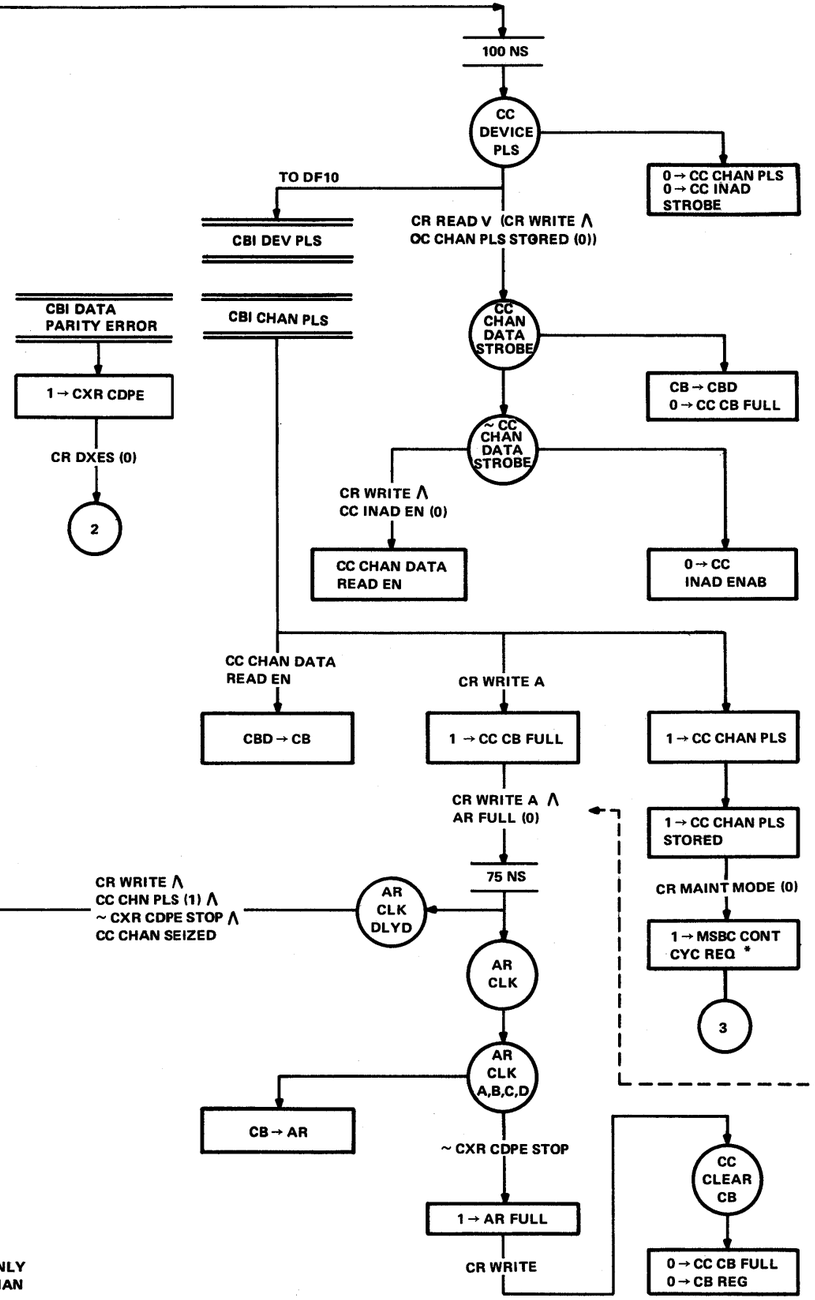
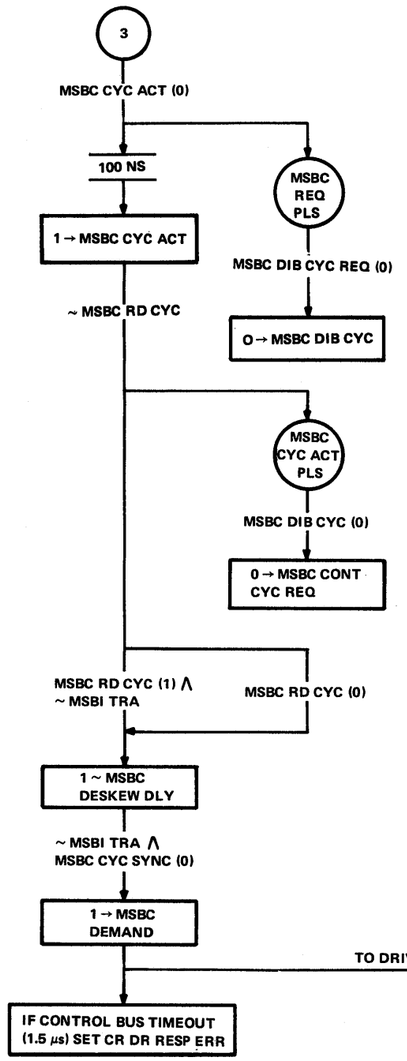


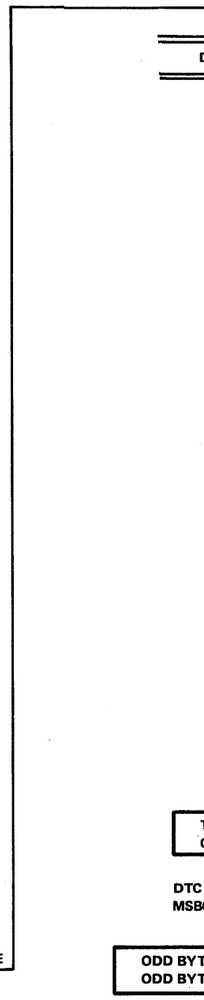
Figure 5-2 DIB Read Cycle Flow Diagram











*MSBC CONT CYC REQ IS SET ONLY ON THE TRANSITION OF CC CHAN PLS STORED.

100 NS

CC DEVICE PLS

TO DF10

CBI DEV PLS

CBI CHAN PLS

0 → CC CHAN PLS
0 → CC INAD STROBE

CR READ V (CR WRITE Λ CC CHAN PLS STORED (0))

CC CHAN DATA STROBE

CB → CBD
0 → CC CB FULL

~ CC CHAN DATA STROBE

CR WRITE Λ CC INAD EN (0)

CC CHAN DATA READ EN

0 → CC INAD ENAB

CC CHAN DATA READ EN

CBD → CB

CR WRITE A

1 → CC CB FULL

1 → CC CHAN PLS

CR WRITE A Λ AR FULL (0)

1 → CC CHAN PLS STORED

CR MAINT MODE (0)

1 → MSBC CONT CYC REQ *

3

Λ
3 (1) Λ
E STOP Λ
EIZED

AR CLK DLYD

75 NS

AR CLK

AR CLK A,B,C,D

CB → AR

~ CXR CDPE STOP

1 → AR FULL

CR WRITE

CC CLEAR CB

0 → CC CB FULL
0 → CB REG

3

MSBC CYC ACT (0)

100 NS

1 → MSBC CYC ACT

~ MSBC RD CYC

MSBC REQ PLS

MSBC DIB CYC REQ (0)

0 → MSBC DIB CYC

MSBC CYC ACT PLS

MSBC DIB CYC (0)

0 → MSBC CONT CYC REQ

MSBC RD CYC (1) Λ ~ MSBI TRA

MSBC RD CYC (0)

1 ~ MSBC DESKEW DLY

~ MSBI TRA Λ MSBC CYC SYNC (0)

1 → MSBC DEMAND

IF CONTROL BUS TIMEOUT (1.5 μs) SET CR DR RESP ERR

TO DRIVE

DEMAND

TRA

FROM DRIVE

~ DIB ATTN REG ADDR Λ MSBC RD CYC (0)

MSBC END CYC PLS

0 → MSBC DEMAND

0 → MSBC CYC ACT

~ MSBC CONT CYC ACT

MSBC CYC ACT (1)

1 → MSBC CYC SYNC

MSBC CONT CYC ACT

1 → MSBC RUN

TO DRIVE

RUN

OCC

FROM DRIVE

IF DATA BUS TIMEOUT (10 MS) SET CR DR RESP ERR

SCLK

FROM DRIVE

TOGGLE DTC ODD BYTE

DTC WRITE ACT
MSBC CONT CYC ACT

ODD BYTE (1) : LD DB FM ARR
ODD BYTE (0) : LD DB FM ARL

TOGGLE DTC EVEN BYTE

MSBI SCLK TE

CC CHAN START EN

DB CLK

DTC ODD BYTE (0) : ARL → DB
DTC ODD BYTE (1) : ARR → DB

DTC ODD BYTE (1) Λ CR WRITE

0 → AR FULL

DTC EVEN BYTE (1) Λ AR FULL (0)

1 → DTC AR DATA SYNC

CC INH (0)
CC CHAN ACTIVE

DTC OVERRUN EN

CR WRITE MSBI SCLK

1 → DTC OVERRUN

2

CC CHAN STOP

DTC TERM

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Figure 5-3 Write Data XFR
Detailed Flow Diagram

50 ns after CC ACTIVE BUF sets, CC CHAN ACT is set if no other device is using the data channel [CC CHAN STARTED (0)]. CC CHAN ACTIVE (1) requests use of the DF10 Data Channel and generates CC CHN START OUT. Since CR WRITE is asserted, and CC CHAN ACT is set, CC SAWRITE OUT is generated to designate a write operation to the DF10. The RH10 now waits for the DF10 to respond with CBI CHN BUSY IN.

5.3.6 CC CHAN ACTIVE

NOTE

In the case where some device has requested the data channel further down the bus, the RH10 logic merely routes the signal to the DF10. The RH10 receives a CBI CHN START IN signal and passes it to the DF10 as a CBI CHN START OUT signal. In addition, the CBI CHN START IN signal generates CC CHN START OUT. This flip-flop, in turn, direct sets the CC CHAN STARTED flip-flop which inhibits the CHAN ACTIVE flip-flop from setting. When the CBI CHN BUSY IN signal is received from the DF10 as a result of some other device, the RH10 merely passes the signal to the requesting device down the bus.

The DF10 Data Channel transmits CBI CHN BUSY IN back to the RH10 when it permits the RH10 to assume control. When the RH10 receives CBI CHN BUSY IN, it has control of the DF10. CBI CHN BUSY IN is gated with CC CHAN ACTIVE (1) to generate CC CHAN SEIZED which indicates that the CBI CHN BUSY IN signal did not result from a request of another device, and ensures that the RH10 has the data channel.

5.3.7 Initial Address

CC CHAN SEIZED performs the following functions:

a. Clears the CC ACTIVE BUF flip-flop.

b. Sets the CC INAD STROBE flip-flop since the BUSY flip-flop is set and the IBC READ IN signal is not asserted at this time.

CC INAD STROBE direct sets CC INAD EN which gates the contents of the CR INAD register (initial address) to the channel bus drivers (see RH10-0-CB). Since CR WRITE is asserted and CC CHAN PLS STORED is still a 0, CC CHAN DATA STROBE is generated, which gates the contents of the channel bus mixers onto the channel bus drivers (see RH10-0-CBD). After a 100-ns delay, the RH10 issues DEV PLS to inform the DF10 that the initial address has been sent. The DF10 strobes the initial address, which contains the address of the first control word. The DF10 then fetches the first data word from memory and prepares to transmit it to the RH10. CC CHAN DATA STROBE, in addition to gating the initial address to the DF10, also clears the CC CB FULL flip-flop. The trailing edge of CC CHAN DATA STROBE clears the CC INAD EN flip-flop, since the initial address has now been sent to the DF10. The DF10 accesses the control word from the initial address and begins to fetch the data words from memory.

5.3.8 Data Transmission

The first data word is received by the bus receivers (see RH10-0-CBD), and is gated into the channel buffer as a result of CC CHAN DATA READ EN being asserted (see RH10-0-CB). The CC CB FULL flip-flop is set indicating that the channel buffer is full. 75 ns after this, AR CLK and AR CLK DLYD are generated if the AR is empty [AR FULL (0)]. This causes the contents of the CB register to be clocked into the AR register and causes the AR FULL flip-flop to set if there is no channel data parity error or if there is a channel parity error, but the Disable Transfer Error Stop (DXES) flip-flop is set which, in effect, disables the parity error. As a result of the transfer of the contents of the CB to the AR, the CC CLEAR CB signal is generated which clears the CB register and clears the CC CB FULL flip-flop.

As a result of AR CLK DLYD a second CC DEV PLS is issued after 100 ns, since CC CHAN SEIZED and CC CHAN PLS (1) are both asserted and the flow loops back to this previously described path. Consequently, this loop ensures that the data words from the DF10 are properly loaded into the CB from the bus receivers and then into the AR. The loop also signals the DF10 when the CB is empty to allow a new data word to be accepted.

5.3.9 Massbus Control Bus Cycle

When the DF10 transmits the first CHAN PLS to the RH10 with the data word, the RH10 sets the CC CHAN PLS flip-flop which, in turn, sets the CHAN PLS STORED flip-flop. The CHAN PLS flip-flop is set each time a CHAN PLS from the DF10 is received and is cleared each time CC DEV PLS is issued. The CHAN PLS STORED flip-flop remains set during the entire data transfer. If the RH10 is not in maintenance mode, CC CHAN PLS STORED sets the MSBC CONT CYC REQ flip-flop which initiates the Massbus cycle.

NOTE

The fact that CHAN PLS STORED is set now inhibits the flow from looping through the INAD branch.

MSBC REQ PLS is generated as a result of MSBC CONT CYC REQ going set. 100 ns after REQ PLS, MSBC CYC ACT is set.

5.3.9.1 Cycle Active Pulse – 100 ns after MSBC CONT CYC REQ is set, MSBC CYC ACT is set, indicating a control cycle is initiated in this case. The setting of MSBC CYC ACT causes MSBC CYC ACT PLS which is ANDed with MSBC DIB CYC (0) to initiate MSBC CONT CYC REQUEST thereby requesting a control cycle on the Massbus.

In addition, the setting of CYC ACT triggers the MSBC DESKEW DLY one-shot if either of the following conditions are present:

1. If the present cycle is a write cycle (~ MSBC CB RD CY) and the previous cycle was a write cycle [MSBC RD CYC (0)], or

2. If the present cycle is a write cycle and the previous cycle was a read cycle [MSBC RD CYC (1)]. In this case, it is necessary to receive TRA from the drive before MSBC DESKEW DLY can be initiated.

5.3.9.2 DEMAND – At the end of 275 ns, MSBC DESKEW DLY times out and sets MSBC DEMAND. The 275-ns deskew allows sufficient time for the control and address lines (asynchronous portion of Massbus) to stabilize. DEM is sent to the drive via the Massbus. Upon receipt of DEM, the drive responds with TRA. If the drive does not respond with 1.5 μs, the flip-flop will cause a CR Drive Response Error (CR DR RESP ERR).

5.3.9.3 End Cycle Pulse – In a write data transfer, MSBC END CYCLE PLS is generated upon receipt of TRA as long as the Attention Summary register is not being addressed. MSBC END CYC PLS clears the MSBC DEMAND flip-flop and the MSBC CYC ACT flip-flop to allow a new cycle to be initiated. The MSBI TRA signal from the drive also sets MSBC CYC SYNC. This inhibits the DEMAND flip-flop from setting again due to a transient. The DEMAND flip-flop is cleared by MSBC END CYC PLS.

5.3.9.4 RUN Signal – If a control cycle is performed (which is true), the RH10 asserts RUN. This signal is transmitted to the drive and informs the drive to prepare for a data transfer. The drive responds with OCC indicating receipt of the RUN signal.

NOTE

If OCC is not received from the drive within 10 ms of RUN, the CXR DBTO flip-flop is set and the CR Drive Response Error (CR DR RESP ERR) is asserted.

5.3.9.5 SCLK Signal – After transmitting OCC to the RH10, the drive issues a Sync Clock (SCLK) signal to the RH10 which echoes back the SCLK as Write Clock (WCLK) along with the data word. the SCLK and trailing edge of SCLK also performs the following functions in the RH10.

1. SCLK toggles the DTC ODD BYTE flip-flop. This flip-flop is ANDed with MSBC CONT CYC ACT. If DTC ODD BYTE is a 1, DTC LD DB FM ARR is generated and if DTC ODD BYTE is a 0, DTC LD DB FM ARL is generated. A four-input multiplexer feeds the data buffer (see RH10-0-DB) – one of the inputs is from the left-half of the AR and one is from the right-half of the AR. Initially, ODD BYTE is a 0, and the left-half (most significant) of the AR is loaded into the DB because the DTC LD DB FM ARL signal is asserted, which places the left-half of the AR at the output of the multiplexer feeding the data buffer. At the leading edge of SCLK, DTC ODD BYTE toggles to a 1, which enables DTC LD DB FM ARR, placing the contents of the right-half of the AR register at the output of the multiplexer. At the trailing edge of SCLK, DB CLK is generated which strobes the output of the multiplexer into the data buffer.

2. The trailing edge of SCLK toggles the DTC EVEN BYTE flip-flop. This flip-flop is set when the right-half of the AR is being transferred to the DB.

5.3.9.6 AR DATA SYNC Signal – If DTC EVEN BYTE is set and AR FULL is on a 0, DTC AR DATA SYNC is set upon receipt of SCLK. DTC AR DATA SYNC accomplishes the following events:

1. Inhibits the DTC LD DB FM ARR and DTC LD DB FM ARL signals which inhibits further transfers from the AR to the DB. This signifies there is no more data to transfer and provides a means of zero filling for a partial sector transfer.

2. Generates DTC OVERRUN EN since the channel is still active [CC CHAN ACTIVE (1)] and CC INH is reset. At the leading edge of the next SCLK, DTC OVERRUN is set. This indicates that there is no data word in the CB and the RH10 is trying to fetch a word from memory and has failed to do so before the receipt of SCLK from the drive.

5.3.9.7 Parity Generation – The DB register is loaded on the trailing edge of SCLK and the drive strobes data on the leading edge. The parity network will compute parity and assert the parity line if necessary prior to the data being strobed by the drive.

5.3.9.8 Write Clock Signal – Each SCLK from the drive is echoed back to the drive as a WCLK from the RH10. The RH10 places a data word on the data portion of the Massbus for each WCLK. The drive strobes the data off the Massbus at the trailing edge of SCLK.

5.4 READ DATA TRANSFER DETAILED DESCRIPTION

The following paragraphs describe a read data transfer operation in detail. The paragraphs are listed in the same order that the sequence of events occur.

5.4.1 Device Selection

The read data transfer is initiated by a DATAO 40_8 instruction which is placed on the I/O bus by the CPU (Figure 5-4). IOS lines 3–9 on the I/O bus specify the RH10 whose address is decoded as 270_8 as shown below:

IOS3	IOS4	IOS5	IOS6	IOS7	IOS8	IOS9
0	1	0	1	1	1	0
						1
	2			7		0

5.4.2 Control Register Select

When the CPU issues the DATAO 40_8 instruction, the Controller Register Select (CR REG SEL) flip-flops are loaded (see RH10-0-IBC). IOBD 00 is a logic 1 and IOBD 01, 02, and 03 are logic 0s. This loads a 40_8 in the CR REG SEL flip-flops. The output of these flip-flops is decoded by the M152 Decoder as IBC CONT REG SEL.

5.4.3 Drive Selection

When the CPU issues the DATAO 40_8 instruction, the selected drive number is loaded in bits 15–17 on the I/O bus.

The CR CLOCK signal strobes the drive select bits (IOBD 15–IOBD 17) into DR SEL flip-flops 00–DR SEL 02 (see RH10-0-CR). This action selects one of eight possible drives which may be incorporated in the system.

5.4.4 CR CLOCK Pulse

The CR CLOCK pulse is used to clock the various flip-flops in the CR register. For a read data transfer, a function code of 71_8 will be loaded, and DTC XFR COMP, IBC CONT REG SEL, and IBC DATAO SET are asserted to generate CR Clock A and CR Clock B (dual-outputs used for loading purposes). The CR CLOCK is also used to generate IBC INITIAL CLEAR which is used to initialize the RH10. In addition, it performs the following functions:

1. Clocks the initial address from the I/O bus to the INAD register (see RH10-0-CR). This address is contained in bits 21–28 of the I/O bus and is loaded in bits 27–34, respectively, of the Initial Address (INAD) register. The INAD address is the starting memory location which contains the first control word.

2. Clocks the function code from bits 30–34 of the I/O bus into the FUNCT CODE register (see RH10-0-CR). The function code specified for a read operation is 70_8 (71_8 with the GO bit set).

3. Clocks bit 35 from the I/O bus into the GO flip-flop. The GO flip-flop must be set in order for a data transfer to occur.

5.4.5 Start of Transfer

The trailing edge of CR CLOCK is applied to a pulse amplifier which generates CR START XFR A and CR START XFR B pulses (two versions for loading purposes), if the GO bit is set. START XFR B sets the CXR BUSY flip-flop if CXR PREV START is not asserted. If CXR PREV START is asserted, the CXR DONE flip-flop is set and the CXR BUSY flip-flop is reset preventing the RH10 from starting a data transfer. CR START XFR A clocks the CC ACTIVE BUF flip-flop set if CC CHAN START EN is asserted. This signal is asserted if the RH10 is not in local mode or if the RH10 is in local mode with the switch panel CHAN EN switch ON. 50 ns after CC ACTIVE BUF sets, CC CHAN ACTIVE is set if no other device is using the data channel [CC CHAN STARTED (0)]. CC CHAN ACTIVE (1) requests use of the DF10 Data Channel and generates CC CHN START OUT. The RH10 now waits for the DF10 to respond with CBI CHN BUSY IN.

NOTE

In the case where some device has requested the data channel further down the bus, the RH10 logic merely routes the signal to the DF10. The RH10 receives a CBI CHN START IN signal and passes it to the DF10 as a CBI CHN START OUT signal. CC CHN START OUT in the RH10 direct sets the CC CHAN STARTED flip-flop which inhibits the CHAN ACTIVE flip-flop from setting. When the CBI CHN BUSY IN signal is received from the DF10 as a result of some other device, the RH10 then merely passes the signal to the requesting device down the bus since CC CHAN ACTIVE is not asserted.

The DF10 Data Channel transmits CBI CHN BUSY IN back to the RH10 when it permits the RH10 to assume control. When the RH10 receives CBI CHN BUSY IN, it has control of the DF10 (since CC CHAN ACTIVE is asserted). CBI CHN BUSY IN is gated with CC CHAN ACTIVE (1) to generate CC CHAN SEIZED which indicates that the CBI CHN BUSY IN signal did not result from a request of another device, and ensures that the RH10 has the data channel.

5.4.6 Initial Address

CC CHAN SEIZED performs the following functions:

1. Clears the CC ACTIVE BUF flip-flop
2. Sets the CC INAD STROBE flip-flop since the BUSY flip-flop is set and the IBC READ IN signal is not asserted at this time.

CC INAD STROBE direct sets CC INAD EN which gates the contents of the CR INAD register (containing the initial address) onto the channel bus mixers (see RH10-0-CB). After a 100-ns delay, CC DEV PULSE is issued to the DF10.

NOTE

Since this is a read data transfer, ~SAWRITE OUT is asserted indicating to the DF10 that a drive-to-memory transfer is to occur.

5.4.6.1 Channel Data Strobe – CC CHAN DATA STROBE is asserted which strobes the initial address from the Channel Bus mixers into the Channel Bus drivers (see RH10-0-CBD), and also clears out the CC CB FULL flip-flop. On the negation of CC CHAN DATA STROBE, the CC INAD EN flip-flop is cleared.

5.4.6.2 Channel Pulse – The RH10, after transmitting the device pulse to the DF10 waits for a CBI CHN BUSY IN signal. This signal sets the CC CHAN PLS flip-flop, which in turn, sets the CC CHAN PLS STORED flip-flop. The CC CHAN PLS flip-flop is cleared each time a DEV PLS is issued by the RH10 and is set each time CBI CHN PLS is received from the DF10, whereas the CC CHAN PLS STORED flip-flop remains set during the entire data transfer.

5.4.7 Massbus Control Bus Cycle

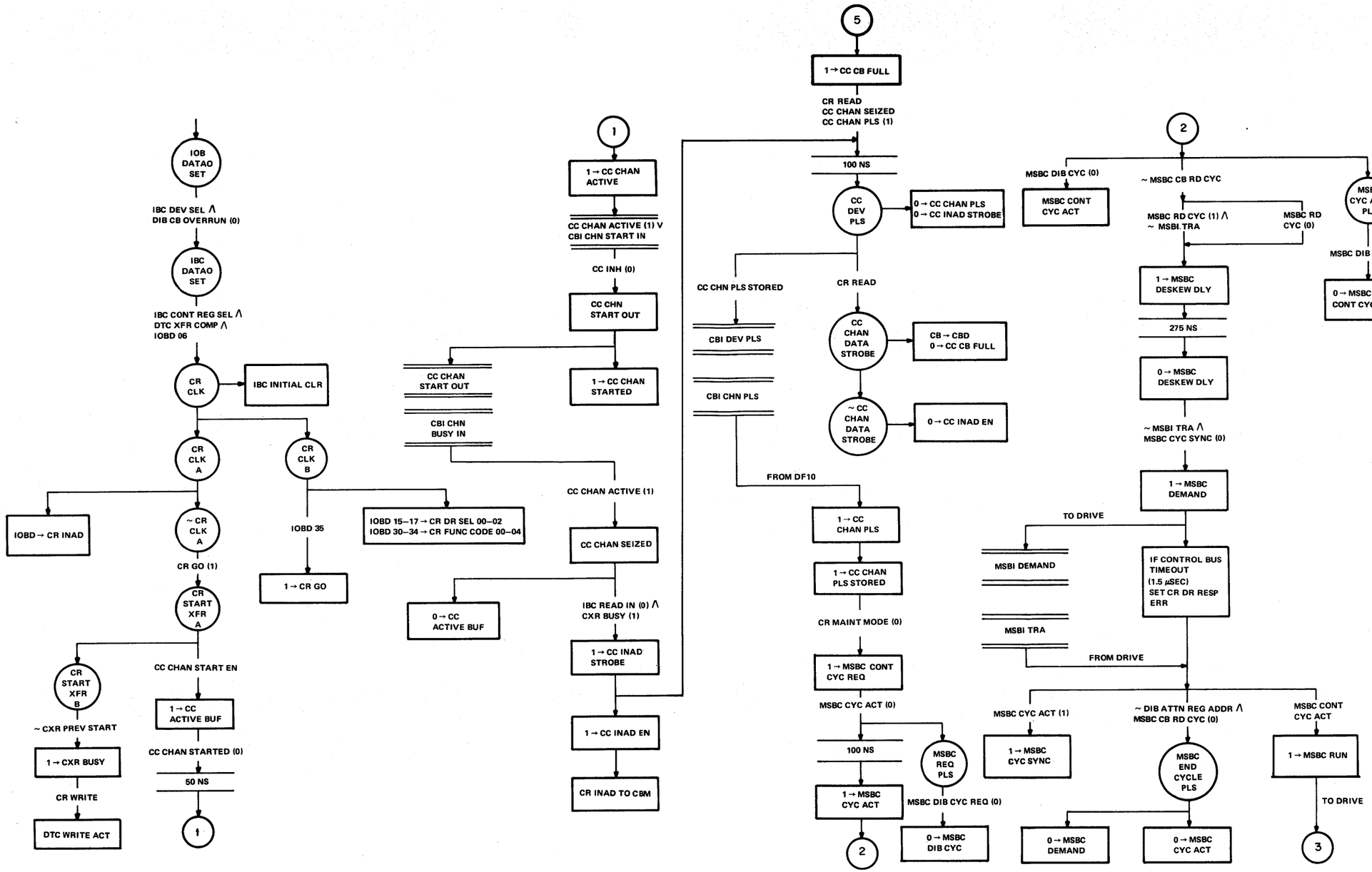
Since the RH10 is not in Maintenance mode, the MSBC CONT CYC REG flip-flop is set. MSBC REQ PLS is generated and clears out the MSBC DIB CYC flip-flop since MSBC DIB CYC REQ has not been set. After a 100-ns delay, MSBC CYC ACT is set.

The setting of MSBC CYC ACT indicates a Massbus cycle will occur and causes the following:

1. Generates MSBC CONT CYC ACT.
2. Fires the 275-ns MSBC DESKEW DLY. This occurs for a read or write operation since MSBC CB RD CYC is not asserted (this signal is asserted only for a DIB read cycle). If the previous cycle was a read [MSBC RD CYC (1)], it is necessary to wait for TRA to be removed from the Massbus before initiating MSBC DESKEW DLY. If the previous cycle was a write cycle, MSBC DESKEW DLY is initiated immediately. The 275-ns deskew allows sufficient time for the address and control lines to settle on the Massbus. After 275 ns, the deskew times out and DEM is asserted on the Massbus provided (1) TRA is not asserted from the previous cycle and (2) the MSBC CYC SYNC flip-flop is cleared.

NOTE

If the drive does not respond to DEM within 1.5 μs, a control bus timeout occurs and sets CR DR RESP ERR.


IOB DATAO SET
IBC DEV SEL Λ DIB CB OVERRUN (0)
IBC DATAO SET
IBC CONT REG SEL Λ DTC XFR COMP Λ IOBD 06
CR CLK
IBC INITIAL CLR
CR CLK A
CR CLK B
IOBD → CR INAD
~ CR CLK A
CR GO (1)
CR START XFR A
CR START XFR B
~ CXR PREV START
1 → CXR BUSY
CR WRITE
DTC WRITE ACT
CC CHAN START EN
1 → CC ACTIVE BUF
CC CHAN STARTED (0)
50 NS
1
1 → CR GO
IOBD 35
IOBD 15–17 → CR DR SEL 00–02
IOBD 30–34 → CR FUNC CODE 00–04
1
1 → CC CHAN ACTIVE
CC CHAN ACTIVE (1) V CBI CHN START IN
CC INH (0)
CC CHN START OUT
1 → CC CHAN STARTED
CC CHAN START OUT
CBI CHN BUSY IN
0 → CC ACTIVE BUF
CC CHAN ACTIVE (1)
CC CHAN SEIZED
IBC READ IN (0) Λ CXR BUSY (1)
1 → CC INAD STROBE
1 → CC INAD EN
CR INAD TO CBM
5
1 → CC CB FULL
CR READ
CC CHAN SEIZED
CC CHAN PLS (1)
100 NS
CC DEV PLS
0 → CC CHAN PLS
0 → CC INAD STROBE
CC CHN PLS STORED
CR READ
CBI DEV PLS
CC CHAN DATA STROBE
CB → CBD
0 → CC CB FULL
CBI CHN PLS
~ CC CHAN DATA STROBE
0 → CC INAD EN
FROM DF10
1 → CC CHAN PLS
1 → CC CHAN PLS STORED
CR MAINT MODE (0)
1 → MSBC CONT CYC REQ
MSBC CYC ACT (0)
100 NS
1 → MSBC CYC ACT
2
MSBC REQ PLS
MSBC DIB CYC REQ (0)
0 → MSBC DIB CYC
2
MSBC DIB CYC (0)
MSBC CONT CYC ACT
~ MSBC CB RD CYC
MSBC RD CYC (1) Λ ~ MSBI TRA
MSBC RD CYC (0)
MSBC CYC ACT PLS
MSBC DIB CYC (0)
0 → MSBC CONT CYC REQ
1 → MSBC DESKEW DLY
275 NS
0 → MSBC DESKEW DLY
~ MSBI TRA Λ MSBC CYC SYNC (0)
1 → MSBC DEMAND
TO DRIVE
MSBI DEMAND
IF CONTROL BUS TIMEOUT (1.5 μSEC) SET CR DR RESP ERR
MSBI TRA
FROM DRIVE
MSBC CYC ACT (1)
1 → MSBC CYC SYNC
~ DIB ATTN REG ADDR Λ MSBC CB RD CYC (0)
MSBC END CYCLE PLS
MSBC CONT CYC ACT
1 → MSBC RUN
TO DRIVE
0 → MSBC DEMAND
0 → MSBC CYC ACT
3

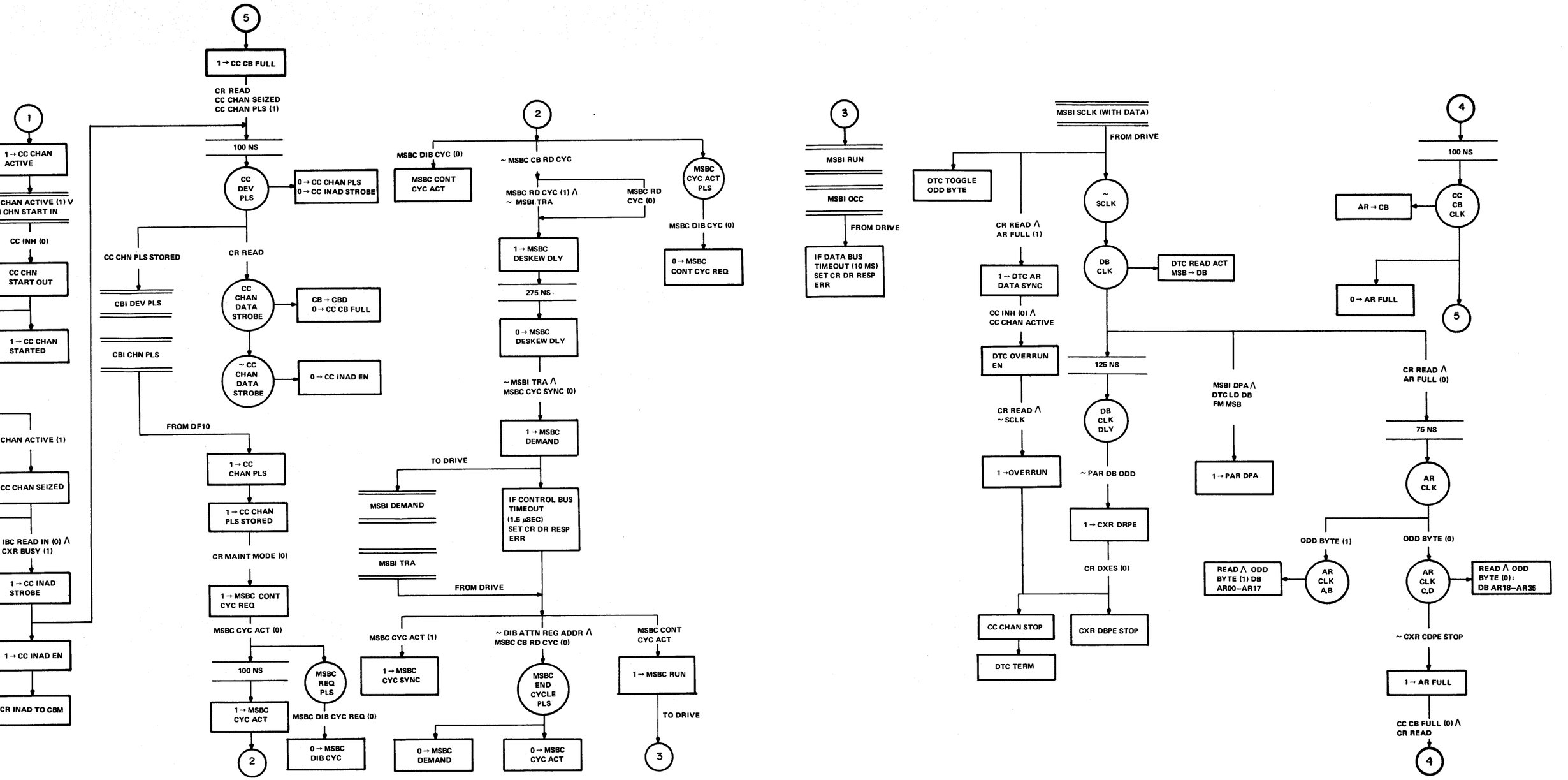


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Figure 5-4 Detailed Read Data Transfer Flow Diagram

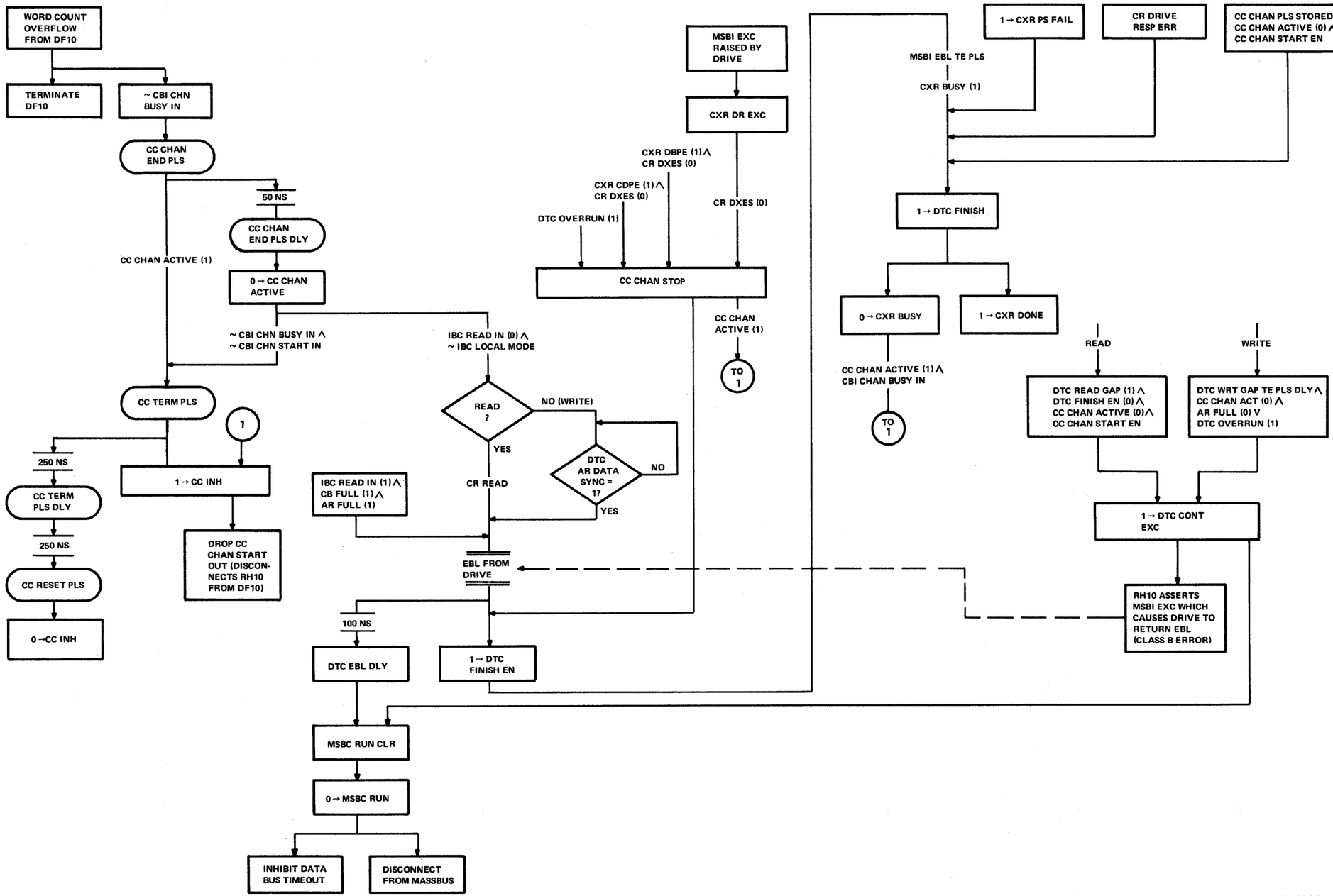


Figure 5-5 Termination Flow Diagram

When the drive responds with TRA, the following events occur in the RH10.

1. The MSBC CYC SYNC flip-flop is set since MSBC CYC ACT is already set.

2. The RUN signal from the RH10 is asserted on the Massbus since MSBC CONT CYC ACT has been asserted and since the drive has responded to the DEM signal from the RH10 by issuing TRA. The drive responds to the MSBI RUN signal by issuing MSBI OCC, indicating that it is ready to send data in this case. If the RH10 does not receive MSBI OCC within 10 ms, a Data Bus Timeout occurs and sets CR Drive Response Error (CR DR RESP ERR).

3. MSBC END CYC PLS is asserted, since the Attention Summary register has not been addressed and since MSBC RD CYC is reset. Note that this flip-flop is set only for a DIB read cycle. MSBC END CYC PLS resets the MSBC DEMAND flip-flop and resets the MSBC CYC ACT flip-flop.

5.4.8 Data Transfer

At this point, the RH10 and the drive are logically connected and are prepared to do a read data transfer. The drive places the first data word on the Massbus accompanied by Sync Clock (SCLK). The fact that CR READ is asserted and the CXR BUSY flip-flop is set causes DTC READ ACT to go true. Since CR MAINT MODE is cleared, DTC LD DB FM MSB is generated. This signal gates the data from the Massbus through the multiplexer, located at the input to the data buffer. The SCLK signal from the drive also causes the DTC ODD BYTE flip-flop to toggle which designates which half of the word is being read from the drive. The trailing edge of SCLK causes the DB CLK signal to occur which clocks the data word from the output of the multiplexer into the data buffer.

NOTE

If the AR is full upon receipt of SCLK from the drive, DTC AR DATA SYNC is set. Since CC INH is reset and the channel is still active (CC CHAN ACTIVE), DTC OVERRUN EN is set which causes DTC OVERRUN to set on the next SCLK, indicating that the drive is over-running the RH10 (transferring words faster than the RH10 can process them).

5.4.8.1 Parity Check – DB CLK DLY is asserted 125 ns after DB CLK and is used to check the data bus parity. If the parity is not odd, the Data Bus Parity Error (CXR DBPE) flip-flop is set. If CR DXES is reset (enabling the error condition), then CXR DBPE STOP is asserted, causing the RH10 to terminate. If the CR DXES flip-flop is set, the error is disabled and the RH10 continues as normal.

If the parity bit from the Massbus is asserted, it sets the PAR DPA flip-flop at the time of DTC LD DB FM MSB.

5.4.8.2 AR CLK Logic – 75 ns after DB CLK, AR CLK is asserted, provided the AR is empty. This inhibits the AR from being loaded while there is still a word in the AR. Depending on the state of the DTC ODD BYTE flip-flop, AR CLK A, B, C and D is generated. If DTC ODD BYTE is a 1, AR CLK A and AR CLK B are generated. If DTC ODD BYTE is a 0, AR CLK C and AR CLK D are generated. The AR CLK A and AR CLK B signals are used to load the left-half of the AR (bits 00–17) and the AR CLK C and AR CLK D signals are used to load the right-half of the AR (bits 18–35).

If there is no Channel Data Parity Error (not asserted on a read operation), the AR CLK D signal causes the AR FULL flip-flop to set. At this point, both the left-half and the right-half of the AR have been loaded. When the AR is filled and the CB register is empty (during a read data transfer), CC CB CLK is generated after a 100-ns delay. This signal clocks the contents of the AR into the CB and clocks the CC CB FULL flip-flop set. In addition, CC CB CLK clears the AR FULL flip-flop during a read data transfer. Now the AR is ready to accept another word from the data buffer and the AR FULL flip-flop is cleared so it can set when the AR is loaded with a new data word. 100 ns after the CB is loaded, the RH10 issues a DEV PLS to the channel. This signal is issued to the DF10 Data Channel. CC DEV PLS also generates CC CHAN DATA STROBE which gates the contents of the CB register onto the channel bus. The CC CB FULL flip-flop is cleared and the CB is ready to accept another word from the AR. When the next data word is received, the CC CB FULL flip-flop is set and when the word is sent to the DF10, the CC CB FULL flip-flop is cleared.

5.5 RH10 TERMINATIONS

The RH10 can normally terminate at the completion of a data transfer or can abnormally terminate under a variety of error conditions, including DF10 error conditions, RH10 error conditions, and drive error conditions. The drive error

conditions can be either a Class A error (non-fatal) or a Class B error (fatal) condition. The following paragraphs describe the normal terminations and the abnormal terminations. Figure 5-5 is a flow diagram showing the various termination paths.

5.5.1 Normal Terminations

Normal termination is initiated by the sensing of word count overflow in the DF10 Data Channel. This action causes the DF10 to terminate and drops the CBI CHN BUSY IN signal to the RH10. This signal asserts CC CHN END PLS which is ANDed with CC CHAN ACTIVE (1) to assert CC TERM PLS. CC TERM PLS sets CC INH which disconnects the RH10 from the DF10. 250 ns after CC TERM PLS, CC TERM PLS DLY is asserted and 250 ns after CC TERM DLY is asserted, CC RESET PLS is asserted, which resets the CC INH flip-flop.

CC CHAN END PLS, in addition to asserting CC TERM PLS, is also delayed 50 ns and asserts CC CHAN END PLS DLY, which clears the CC CHAN ACTIVE flip-flop.

If the RH10 is performing a write data transfer, DTC AR DATA SYNC must be set and an EBL from the drive must be received before normal termination can occur. The setting of DTC AR DATA SYNC indicates that both the CB and the AR are empty, consequently, this prevents the RH10 from terminating while it still has words to transfer to the drive.

If the RH10 is performing a read data transfer, DTC FINISH EN is set upon receipt of an EBL pulse from the drive.

If the RH10 is doing a read-in operation, IBC READ IN must be set, the CB and the AR must be filled with the last two words from the drive, and EBL must be received before DTC FINISH EN is set. The read-in operation is described in Paragraph 5.8.

100 ns after EBL, DTC EBL DLY is asserted and is ANDed with DTC FINISH EN to generate MSBC RUN CLR which direct clears the RUN flip-flop, disconnecting the RH10 from the synchronous Massbus.

When the trailing edge of EBL occurs, DTC FINISH is set (CXR BUSY still being set at this time). The setting of DTC FINISH clears the CXR BUSY flip-flop and sets the CXR DONE flip-flop to terminate the RH10.

To summarize, the word count overflow in the DF10 caused the DF10 to disconnect from the RH10. The RH10, in turn, disconnects from the drive and the RH10 sequences through its shut-down logic to terminate the operation.

5.5.2 Abnormal Terminations

The RH10 can terminate due to a variety of conditions occurring in the drive, in the RH10, or in the DF10. These abnormal termination conditions are described in the following paragraphs.

5.5.2.1 DTC OVERRUN Flip-Flop – The DTC OVERRUN flip-flop can be set under two conditions – one being where the drive is transferring words to the RH10 at a rate faster than the DF10 is accepting them from the RH10 (read overrun) and the second being where the DF10 is transferring words to the RH10 at a slower rate than the drive is requesting them from the RH10 (write overrun).

For the read overrun condition, the DTC AR DATA SYNC flip-flop is set on the leading edge of SCLK if the AR FULL flip-flop is set. Since CC INH is negated and CC CHAN ACTIVE is set, DTC OVERRUN EN is set. This condition causes DTC OVERRUN to set on the trailing edge of SCLK.

For the write overrun condition, DTC AR DATA SYNC is set as a result of DTC EVEN BYTE (1), indicating the last half of the data word has been strobed into the DB and AR FULL (0), (no data is available to the drive). Under these conditions, the DTC AR DATA SYNC is set upon receipt of the next SCLK. This causes DTC OVERRUN EN to be asserted since CC INH is negated. CC CHAN ACTIVE is asserted at this time. DTC OVERRUN EN causes DTC OVERRUN to set upon receipt of the trailing edge of SCLK.

If DTC OVERRUN is set during a mid-sector, the data transfer will continue until the end of the current sector. The DF10 is terminated immediately when the overrun condition is sensed. If an overrun is detected on a write operation, the rest of the sector will be zero-filled. If an overrun is detected on a read or write between sectors, DTC CONT EXC will be asserted to terminate the drive.

5.5.2.2 Channel Bus Data Parity Error – A Channel Bus Data Parity Error causes the CXR CDPE flip-flop to set. If CR DXES is reset, indicating that the error condition is to terminate the RH10, CC CHAN STOP is generated, which sets CC INH to allow the RH10 to disconnect from the DF10. DTC FINISH EN is set upon receipt of EBL and DTC FINISH is set on the trailing edge of EBL, which causes CXR BUSY to clear and CXR DONE to set.

5.5.2.3 Data Bus Parity Error – A data bus parity error causes the CXR DBPE flip-flop to set upon generation of DB CLK DLY. If CR DXES is reset, indicating that the error condition is to terminate the RH10, CC CHAN STOP is generated, which sets CC INH, to allow the RH10 to disconnect from the DF10. DTC FINISH EN is set upon receipt of EBL and DTC FINISH is set on the trailing edge of EBL, which causes CXR BUSY to clear and CXR DONE to set.

5.5.2.4 Drive Exception – If the drive should assert the EXCEPTION line due to a drive error, the CXR DR EXC flip-flop is clocked set if CXR BUSY is set (indicating a data transfer in progress). If CR DXES is reset, indicating that the error condition is to terminate the RH10, CC CHAN STOP is asserted. CC CHAN STOP sets CC INH to allow the RH10 to disconnect from the DF10. DTC FINISH EN is set upon receipt of EBL and DTC FINISH to set on the trailing edge of EBL, which causes CXR BUSY to clear and CXR DONE to set.

5.5.2.5 Power Supply Fail – If a low voltage condition is detected by the CXR LOW VOLT DETECTOR, a CXR PS FAIL signal is generated, which sets DTC FINISH. This causes CXR BUSY to reset and CXR DONE to set, terminating the RH10.

5.5.2.6 Drive Response Error – If there is a control bus timeout or a data bus timeout on the Massbus, the CR DR RESP ERROR flip-flop is set indicating a non-existent drive or an improperly addressed drive. This sets DTC FINISH which clears CXR BUSY and sets CXR DONE to terminate the RH10.

5.5.2.7 DF10 Terminates Before CHAN PLS STORED – If the DF10 terminates before the RH10 receives the first channel pulse (i.e., control parity error on initial control word fetch), CHN BUSY IN is generated which direct resets CC CHAN ACT, causing DTC FINISH to set which clears CXR BUSY and sets CXR DONE.

5.6 KA10 AND KI10 INTERRUPT LOGIC

The RH10 interrupt logic is shown on logic print RH10-0-IADR. The KI10 INTR flip-flop, when set, designates a KI10 interrupt and, when reset, designates a KA10 interrupt. The flip-flop is set by a 1 in IOBD 16 and is clocked by IBC DATAO set, IOBD 06 (load register) and IBC IADR REG SEL (which selects the interrupt address register by loading 44_8 in the CR).

5.6.1 KA10 Interrupt

For a KA10 interrupt, IOBD 16 is set to a 0 and the Priority Interrupt Address (PIA) is set via a CONO instruction from the KA10. The PIA from bits 33–35 of the CONO are transferred to three PIA flip-flops in the RH10 (see RH10-0-IADR). When a Register Access Error, an attention condition, a control bus overrun, or a done condition occurs and the RH10 is not in local mode, the PIA is decoded in the RH10 and raises the priority level on the assigned channel (IADR PI REQ 1 – IADR PI REQ 7). When the CPU recognizes the PI level, it will interrupt to a subroutine whose address is calculated as 40 plus 2 times the channel number.

5.6.2 KI10 Interrupt

The KI10 priority interrupt operates in a similar fashion to the KA10. In addition to the priority interrupt, the KI10 can do a vector interrupt. The procedure for a vector interrupt is initiated by a CONO instruction from the KI10 which sets up a PIA in the RH10 just as in the case of a KA10 priority interrupt. A DATAO is then issued by the KI10 to load the vector address in the Interrupt Address register and to set the KI10 INTR flip-flop via IOBD 16. The vector address is loaded from IOBD 27–IOBD 35 into IADR 27–35, respectively. When the error or done condition raises an interrupt and the RH10 is not in local mode, the PIA is decoded and sent to the processor. When the processor recognizes the priority level, it asserts IOB PI REQ SYNC, along with the channel number of the request it is going to service. The channel number is transferred to a comparator in the RH10 via I/O bus bits 00–02. The comparator compares these bits with the PIA bits initially set in. If the two compare, then the RH10 is the device causing the interrupt and IADR PI EQUAL is asserted. The IOB PI REQ SYNC signal from the CPU sets the IADR PI REQ SYNC flip-flop which is ANDed with PI EQUAL to generate IADR PI RDY. The CPU then issues IOB PI GRANT IN BUS which is ANDed with PI RDY to generate PI START which is the gating signal used to strobe the vector address onto the I/O bus via the I/O status mixers (see RH10-0-ISM 5 and 6). In addition, the IADR PI GRANT OUT BUS signal is inhibited to prevent the GRANT from being passed to the next device. If the RH10 did not cause the interrupt, IADR PI RDY is inhibited, which enables the IOB PI GRANT IN BUS to be passed to the next device on the bus as IADR PI GRANT OUT BUS.

When the vector address is gated onto the I/O bus, a function code designating a KA10 or KI10 type interrupt is also gated onto the I/O bus. The logic for this is shown on RH10-0-ISM1.

The bits designated ~ISM4 and ~ISM5 specify the function code. For a KA10-type interrupt, the KI10 INTR flip-flop is reset and IADR PI START is enabled, causing ~ISM STATUS 04 to be low and ~ISM STATUS 05 to be high, yielding a function code of 01 for a priority-type interrupt. If a KI10-type interrupt is attempted, the KI10 INTR flip-flop is set and IADR PI START is enabled, which causes ~ISM STATUS 04 to be high and ~ISM STATUS 05 to go low, designating a function code of 2_8 for a vector interrupt. The function code is read upon assertion of PI START along with the vector address if a vector-type interrupt is to be performed.

5.7 RH10 MAINTENANCE PANEL

The RH10 maintenance panel (switch panel) allows the RH10 to operate in on-line mode (normal operation) or in local mode. In local mode, the RH10 is under control of the switch panel. Selection of the LOCAL position of the LOCAL/REMOTE switch, causes the IBC LOCAL flip-flop to set indicating Local Mode if no prior cycle is in progress. Figure 5-6 shows a flow diagram of the switch panel logic. Depressing the STOP pushbutton causes the IBC LOCL STOP flip-flop to set, indicating that the cycle will stop at the end of the current local DATAO. When the START switch is depressed, it causes IBC LOCL STRT to set if IBC LOCL STOP is set. This ensures that the RH10 is stopped before it is started. If it is not in a stopped condition, the START pushbutton has no effect.

Depressing the START pushbutton sets IBC LOCL STRT, which in turn, generates IBC LOCL STRT PLS. If the LOCAL/REMOTE switch is in LOCAL, the IBC LOCL STRT DLY one-shot starts to timeout for 440 ns. This signal sets the IBC LOCL DATAO CLR flip-flop at the beginning of the timeout and sets IBC LOCL DATAO SET 440 ns later, after the one-shot has timed out. The IBC LOCL timer one-shot is first fired by the IBC LOCL DATAO CLR flip-flop for 220 ns and when it times out, it asserts the IBC CLEAR PLS which clears IBC LOCL DATAO CLR if IBC LOCL STRT DLY is still set (see timing waveshapes in Figure 5-6). Then 220 ns later, the timer is again fired by the IBC LOCL DATAO SET pulse. At the end of 220 ns, the IBC LOCL TIMER times out and a second IBC CLEAR PLS is asserted which clears the IBC LOCL DATAO SET flip-flop.

The IBC CLEAR PLS is applied to the IBC CONT REG XFR flip-flop. This flip-flop is normally cleared if an RH10 register transfer is to be recycled. IBC CONT REG XFR clears upon receipt of the first IBC CLEAR PLS except if the RH10 control register is selected with the GO bit set (indicating a data transfer). The output of the IBC CONT REG XFR flip-flop is ANDed with MSBC CYC ACT (0) and DTC XFR COMP to assert IBC CYCLE COMP, indicating completion of the cycle. In the case of recycling RH10 register transfers, IBC CONT REG XFR is going to assert IBC CYCLE COMP (the other two inputs being enabled). In the case of recycling drive register transfers, MSBC CYC ACT (0) is going to assert IBC CYCLE COMP (the other two inputs being enabled). In the case of a data transfer, DTC XFR COMP is going to assert IBC CYCLE COMP (the other two inputs being enabled).

When IBC CYCLE COMP fires, it causes the IBC RECYCLE one-shot multivibrator (1 μs) to fire. IBC RECYCLE generates IBC RECYCLE PLS to start another cycle if IBC LOCL STOP is reset. If IBC CR SEL $\wedge$ GO is asserted (indicating a data transfer operation) and IBC LOCL STOP is a 0, the MSBI INIT one-shot will fire for 400 ns. This will generate MSBI INIT to the Massbus.

5.8 READ-IN MODE

The READ-IN feature of the RH10 permits a block of data (bootstrap loader program) to be read from a drive in order to permit peripheral devices, connected to the RH10, to bootstrap the system.

Initially, the operator selects the RH10 by setting 270_8 into the READ IN DEVICE switch on the central processor and sets the READ IN octal thumbwheel switch on the RH10 maintenance panel to the logical address of the drive from which the data will be read. When the CPU READ-IN switch is depressed, an IOB RESET signal is issued which clears all error status flags and initializes the RH10 and associated drives. The READ-IN performs the following operations:

1. A DIB cycle is performed to load the READ-IN preset command (21_8) into register 0 of the selected drive.

2. A control cycle is performed to load the READ command (71_8) into register 0 of the selected drive to initiate a data transfer read operation. The block of data representing the bootstrap loader program is transferred to memory from the drive.

3. Upon normal termination by the DF10, two additional words are read from the disk. The next to last word is the BLKI pointer which is sent to the processor to allow the 'execute' word to be read in via the I/O bus. The BLKI pointer should have a word count of minus 1 to signal the processor to do one DATAI instruction. This DATAI collects the last word read from the disk and is executed by the CPU.

The following paragraphs describe how this is implemented by the READ-IN logic (refer to Figure 5-7).

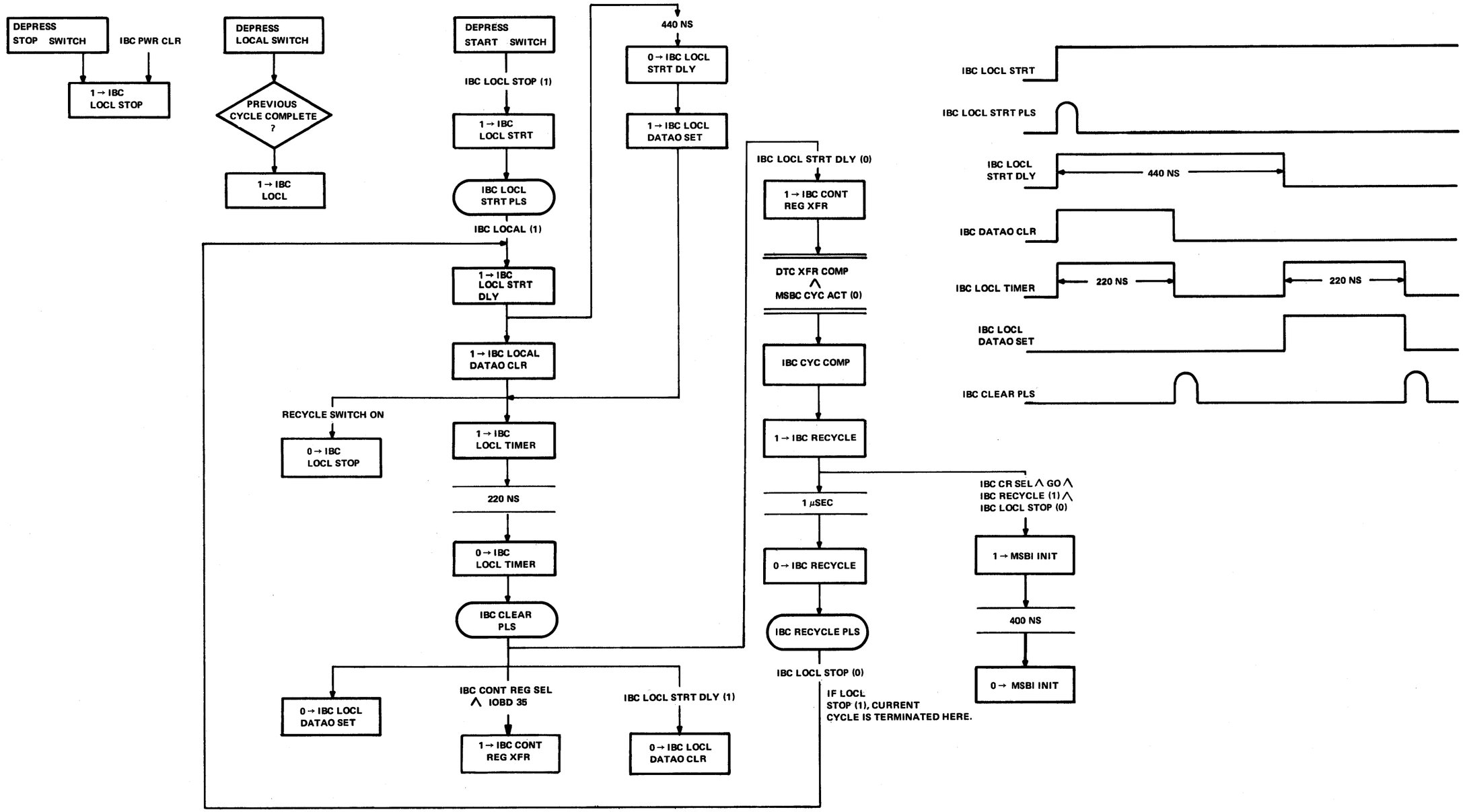


Figure 5-6 Switch Panel Logic Flow Diagram

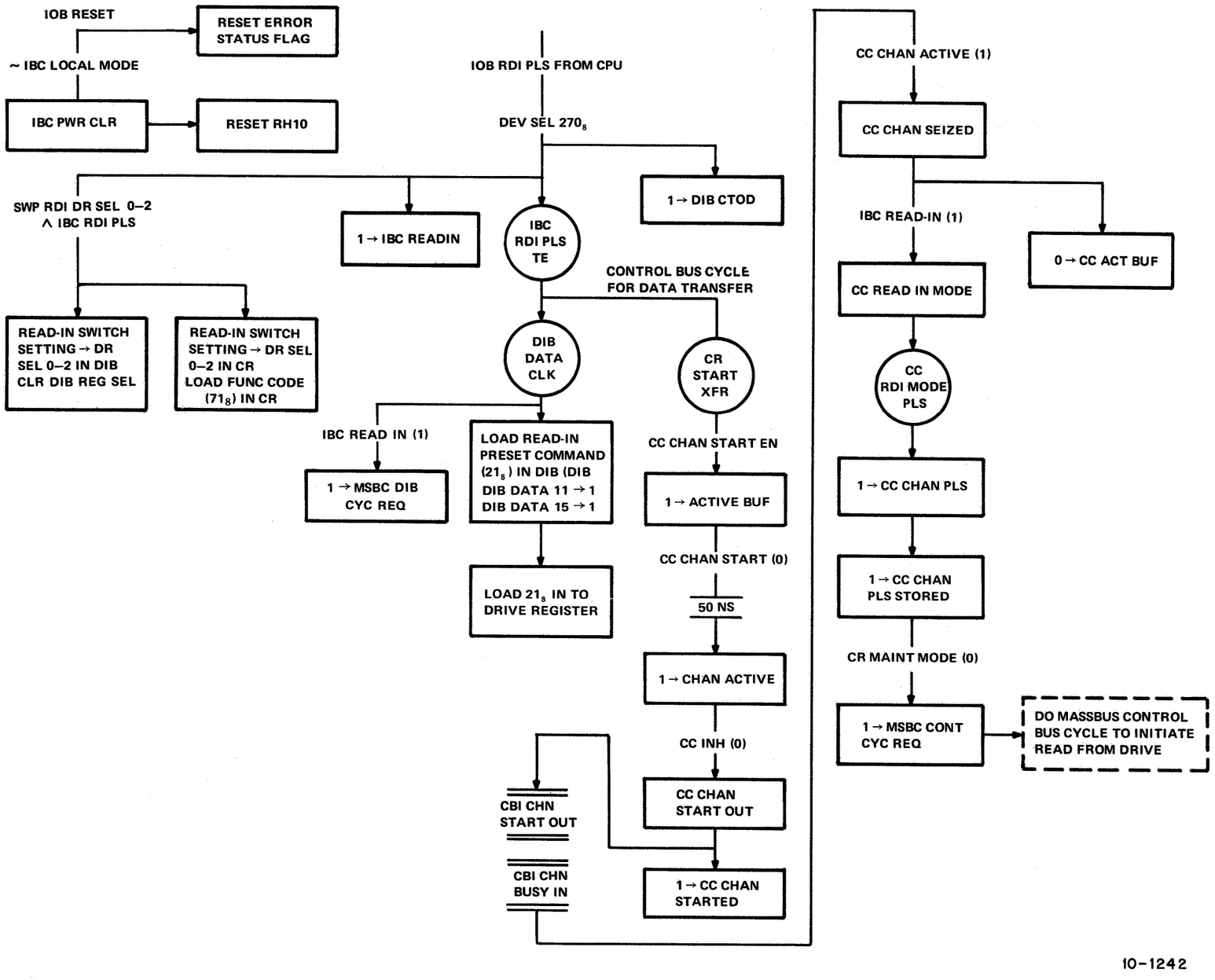


Figure 5-7 READ IN Mode Flow Diagram

5.8.1 DIB Cycle

When the READ-IN switch on the central processor is depressed, an IOB RESET signal is issued by the central processor. IOB RESET asserts IBC PWR CLR which is used to initialize the RH10 and also generates MSBI MB INIT (Massbus Initialize) to initialize the drives.

In addition, an IOB RDI PLS is generated by the CPU and is ANDed with the RH10 device select code of 270_8. This signal causes the following events to occur:

1. It causes the READ-IN thumbwheel switch setting to direct set the DIB and CR register drive select flip-flops. Assume that drive 0 has been selected. Consequently, when the DIB cycle and control cycle is performed, drive 0 will be addressed.

2. It causes the IBC READ-IN flip-flop to set which initiates the DIB cycle (Paragraph 5.2). DIB CTOD is asserted, denoting that a DIB write cycle is to occur. The trailing edge of IBC READ-IN asserts DIB DATA CLK which clocks the READ-IN PRESET command into the DIB register. The DIB cycle then transfers the READ-IN PRESET to drive 0, register 0.

3. IBC RDI PLS TE will also start the DF10 and when CBI CHN BUSY is received, MSBC CONT CYC REQ will be generated, similar to a normal read operation.

The sequence to enable the channel and to do the control cycle differs somewhat from the typical sequence in a normal data transfer and is described in the following paragraphs.

5.8.2 Channel Enable and Massbus Control Bus Cycle

IBC RDI PLS TE asserts CR START XFER which sets CC ACTIVE BUF. If the data channel is free, CC CHAN ACTIVE is set, thus asserting a CC CHN START OUT. This signal clears CCA IDLE in the DF10. The data channel issues CBI CHN BUSY IN when it grants control of the channel to the RH10. CB1 CHN BUSY IN asserts CC CHAN SEIZED which clears the CC ACTIVE BUF flip-flop. At this point, IBC READ IN (1), set by IBC RDI PLS, asserts CC READ IN MODE which (1) sets the CCA READ IN flip-flop in the DF10 and (2) generates CC RDI MODE PLS in the RH10 via a pulse amplifier. CC RDI MODE PLS sets CC CHAN PLS. Note that in a normal data transfer, CC CHAN PLS is set by the DF10, whereas in READ IN, it is set by the RH10. CC CHAN PLS, in turn, sets CC CHAN PLS STORED. CC CHAN PLS toggles with every CC DEV PLS, whereas CC CHAN PLS STORED remains asserted for the entire data transfer. CC CHAN PLS stored sets MSBC CONT CYC REQ to initiate the Massbus control bus cycle. This action initiates a read data transfer.

5.8.3 Massbus Data Bus Cycle

After completion of the control cycle, the data bus cycle is initiated (by the RH10 issuing RUN and the drive returning OCC). The RH10 now waits to receive SCLK signals from the drive. The drive sends the first SCLK, accompanied by the first data word. This first data word from the drive is treated as a valid control word, containing a word count and data address, whereas in the normal data transfer, the first control word is fetched from memory. The control word from the drive is strobed into the DB, the AR, the CB, and is then transmitted to the DF10, accompanied by a DEV PLS. The DF10 receives the control word and loads it into the MB. CC DEV PLS is delayed by the DF10, CCB VCW (valid control word) is set and CIA INAD SYNC in the DF10 is cleared. Successive data words from the drive are transferred to memory in the normal manner. When word count overflow is detected in the DF10, the CCC CWRDRQ flip-flop is set and when CCC END MC is received from the last memory cycle, CCA IDLE is reset and a control word is written in shadow memory. When the DF10 Data Channel shuts down, the RH10 will read two more words from the drive. The first of these words is a BLKI pointer.

5.8.4 BLKI Pointer

The BLKI pointer contains a word count (two's complement) and current address (-1). For READ-IN, word count should be set to 1, which signals the processor to do one additional DATAI instruction. This DATAI instruction collects the word following the BLKI pointer and is the first instruction executed by the program.

The BLKI pointer is transferred from the drive to the DB, the AR and then to the CB. This is followed by the last word, which is transferred from the drive to the DB and to the AR. At this point, the CB and the AR are both full and the channel is inactive [CC CHAN ACTIVE (0)] forcing DTC TERM to be asserted. When the RH10 receives MSBI EBL from the drive, DTC FINISH EN is set, which sets DTC FINISH. Setting of DTC FINISH clears CXR BUSY and sets CXR DONE. CXR BUSY (0) and CC CHAN ACTIVE (0) assert DTC XFR COMP (Transfer Complete) which causes DTC RDI DONE to be asserted. This signal sets the IBC RDI DATA RDY flip-flop, which is transmitted to the CPU as IOB RDI DATA RDY, indicating that the RH10 has a data word ready. This word is the BLKI

pointer, which contains a word count of 1 and a data address of -1, and designates that the CPU is to perform one more DATAI instruction. The CPU issues a DATAI to collect the BLKI pointer. The IBC DATAI signal from the CPU sets the IBC RDI DATAI flip-flop. The trailing edge of RDI DATAI clears the CB FULL flip-flop, and clears the IBC RDI DATA RDY flip-flop. The IBC RDI DATAI flip-flop remains set. Since the AR is full, with the word following the BLKI pointer, and the CB is empty, CC CB CLK is generated. This clocks the contents of the AR into the CB and sets the RDI DATA RDY flip-flop, indicating another word is ready for the CPU.

NOTE

As a result of the BLKI pointer, the CPU is directed to do a second DATAI to collect this last word from the RH10. The CPU consequently takes the last word which is normally a "jump" to the bootstrap loader program.

The second DATAI from the CPU causes the IBC RDI DATAI flip-flop to be clocked clear. This signal direct clears the IBC RDI DATA RDY flip-flop. The trailing edge of the DATAI signal (~IBC RDI DATAI) from the CPU asserts IBC END RDI PLS, which direct clears IBC READ-IN and IBC RDI DATAI to terminate the READ-IN operation.

5.9 REGISTER ACCESS ERROR

One of four types of errors can occur at the end of a DIB cycle (see RH10-0-DIB, sheet 1). These errors are Control Bus Timeout, Control Bus Parity Error, Data Late and Illegal Command. These errors are described in the following paragraphs.

5.9.1 Control Bus Timeout (CBTO)

This error occurs when the drive does not respond to the DEM signal from the RH10. Normally, the drive responds to DEM by issuing TRA, provided the Attention Summary register has not been addressed. The DEM signal initiates a 1.5 μs timeout (see RH10-0-MSBC), which is applied to a pulse amplifier to create CBTO DLY PLS. This signal clocks the CBTO flip-flop set if the RH10 is doing a DIB cycle and the error was not caused by an Attention Summary register.

5.9.2 Control Bus Parity Error (CBPE)

This error occurs if the program tries to read a drive register and a parity error occurs (~PAR CB ODD). LD DIB DATA DLY clocks the CBPE flip-flop set in this case. This signal is asserted upon receipt of TRA from the drive if the Attention Summary register was not addressed.

5.9.3 DATA LATE

This error occurs when the programmer issues a DATAI instruction and the RH10 still has DIB CYC ACT asserted, indicating the read of the drive register has not completed. This condition causes the DIB DATA LATE flip-flop to set.

5.9.4 Illegal Command (ILL COM)

This error occurs when the program tries to write a data transfer function code in the Control register in the drive. For example, if the programmer issued a DATAO with register 0 selected, IOBD 6 (Load register) asserted and a read or write function code specified, the ILL COM flip-flop will set.

5.9.5 RAE Interrupt Logic

The four error conditions described above are ORed on RAE and fed to a pulse amplifier whose output is RAE SET. RAE SET is the enable input to a decoder which decodes the 3-bit drive select code. The output of the decoder is an RAE SET signal for the associated drive causing the error. For example, if drive 00 caused a Register Access Error, RAE SET 00 is asserted. This signal direct sets the RAE flip-flop associated with drive 00. This flip-flop is designated RAE 00. The eight RAE flip-flop outputs are ORed to yield RAE which is asserted in bit 29 of the CONI instruction and which initiates an interrupt (if the RAE EN bit in bit 29 of the CONO instruction is set). Subsequent DIB cycles are blocked; however, control cycles can still occur. If RAE EN is unasserted, the interrupt will not be generated. This action is shown on RH10-0-DIB, sheet 1. When a Register Access Error occurs and RAE EN is set, the circuitry that generates the DIB CLK is inhibited.

The programmer can ascertain which drive caused the error by reading the RAE register and monitoring bits 28–35 in this instruction. In order to clear the RAE flip-flop, the programmer will issue a DATAO 54 and set the IOBD bit corresponding to the desired RAE flip-flop. Note that IBC DATAO SET, IOBD 06 (Load Register) and IBC RAE REG SEL must be present with the IOBD bit set to clear the flip-flop.

5.10 PARITY LOGIC

The parity logic is shown on RH10-0-PAR and is divided into three parts:

1. The parity logic for the control bus portion of the Massbus (shown on the right-hand side)

2. The parity logic for the data bus portion of the Massbus (shown on the left-hand side)

3. The parity logic for writing the CR register (shown below the control bus parity logic).

The parity logic for the control bus and the data bus includes both parity generation logic (for a write operation) and parity checking logic (for a read operation). The parity logic for writing the CR register (PAR CR ODD) only includes parity generating logic (when the drives CR register is written via a MSBC CONT CYC REQ).

5.10.1 Parity Generation Logic (Control Bus)

The parity generation logic for the data bus is similar to the parity generation logic for the control bus; therefore, the control bus logic will be described in detail and differences between the control bus and data bus will be pointed out in subsequent paragraphs. During a write operation, the CPA (parity) flip-flop in the RH10 is cleared because MSBC DIB CYC ACT is unasserted during the DIB DATA CLK pulse.

Correct parity in the RH10 is odd parity and is indicated by the assertion of PAR DIB ODD. During a write, an odd number of logical 1 bits fed into the parity tree will cause PAR DIB ODD to be asserted. The inputs to the parity tree are DIB data bits 00–15 from the DIB data register. For example, assume that an odd number of bits is applied to the upper-half of the parity tree (DB00–DB07) and an even number of bits is applied to the lower-half of the parity tree (DB08–DB15). The output of the upper-half of the parity tree is low and the output of the lower-half of the parity tree is high. The low and high inputs are applied to an exclusive OR gate, which produces a low output when the exclusive OR condition is satisfied. This causes PAR DIB ODD to be asserted, indicating an odd number of bits from the DIB data register.

NOTE

For a write, the AND/NOR Gate whose inputs are PAR CPA (1), (0) and DIB GEN EVC (0), 1 is high which enables a second AND/NOR gate to create PAR DIB ODD. PAR DIB ODD, in turn, is ANDed with MSBC DIB CYC ACT. If the number of bits from the DIB data register is odd, PAR CB ODD is generated, indicating correct parity and, therefore, the parity bit is inhibited. If PAR CB ODD is not asserted (indicating an even number of bits), then ~PAR DIB ODD is generated. This signal is ANDed with MSBI CB WRT EN and causes a 1 to be written into the drives' CPA (parity flip-flop) via the Massbus. The parity checking logic in the drive will check parity generated in the RH10 and will raise a parity error if parity is even. The AND/NOR gate provides a means of checking the RH10 and drive parity checking logic by inverting the parity bit for both read and write.

5.10.2 Parity Checking Logic (Control Bus)

The parity checking logic for the data bus is similar to that of the control bus; therefore, the control bus parity checking logic will be described in detail and differences between the data bus and control bus will be pointed out. During a read operation, the parity tree also monitors the DIB data inputs just as in a write operation. However, the AND/NOR gate which monitors PAR CPA and DIB GEN EVC is included. In normal mode, DIB GEN EVC (0) is normally asserted high, and the state of the CPA flip-flop, plus the state of the DIB data input lines, are used to determine whether or not PAR DIB ODD is asserted. For example, if the number of 1 bits from the DIB data register are even, the CPA flip-flop in the RH10 should be set.

NOTE

The CPA flip-flop in the RH10 actually stores the state of the Massbus CPA line.

This condition totals up to an odd number of bits and PAR DIB ODD is asserted low. If PAR DIB ODD is not asserted, then a parity error has occurred and PAR CB ODD is generated. This signal is used to set the DIB CBPE (Control Bus Parity Error) flip-flop. The clock input to this flip-flop (MSBC LD DIB DATA DLY) is asserted for a read operation.

When DIB GEN EVC (1) is asserted, the AND/NOR gate monitors the reset output of the CPA flip-flop or, in effect, forces even parity. This action causes the ~PAR CB ODD signal to be asserted and causes the DIB CBPE flip-flop to set.

5.10.3 Parity Generation and Checking (Data Bus)

There are several minor differences between the data bus parity logic and the control bus parity logic. The data bus is an 18-bit bus so an extra exclusive-OR gate is included to monitor bits DB16 and DB17. The exclusive-OR gate which generates PAR DB ODD is equivalent to the AND/NOR gate which generates PAR DIB ODD. In a write operation, PAR DIB ODD is asserted when odd parity is generated. In a read operation, PAR DIB ODD is asserted when the number of 1 bits plus the parity bit (DPA) is odd. The CR GEN EVD (0), (1) is similar to the DIB GEN EVC (0), (1). CR GEN EVD (0) is asserted in normal mode and CR GEN EVD (1) is asserted in diagnostic mode. The DPA (parity) flip-flop can be set from the Massbus during a read

operation just as the CPA parity flip-flop. In addition, when the RH10 is in diskless (diagnostic) mode, parity can be computed for the data from the I/O bus to the data buffer. Wrong parity can be forced by loading IOBD 17 as a 1 when the number of 1 bits from the data buffer is odd or by loading a 0 in IOBD 17 when the number of 1 bits from the data buffer is even.

5.10.4 Parity Generation (CR Register)

When writing the drives' Control register (control cycle initiated by a DATAO 40_8), parity is generated for the function code and GO bit (bits 30–35). If the number of logical 1 bits are even, ~PAR CR ODD is asserted. This bit is ANDed with MSBC CONT CYC ACT and causes ~PAR CB ODD to be asserted. This signal is ANDed with MSBI CB WRITE EN and writes a 1 into the drives' CPA parity flip-flop. If the parity is odd, the CPA flip-flop in the drive stays in the 0 state.

CHAPTER 6
MAINTENANCE

6.1 GENERAL

This chapter describes the RH10 installation procedure, the use of the RH10 maintenance panel, the RH10 indicator panel, and the diagnostic programs available for debugging and isolating malfunctions in the RH10 subsystem.

6.2 INSTALLATION

The RH10 is shipped as a complete and factory-tested unit. When the equipment is received, all modules are in place and all intra-bay cabling has been installed. The unit has been tested extensively while operating as part of a standard PDP-10 system. Figure 6-1 represents a simplified block diagram showing typical RH10 cable connections and cable types.

6.2.1 Special Handling

No special handling procedures are required for the RH10 beyond the normal care afforded any piece of scientific equipment of comparable size and weight. However, particular care should be exercised in the use of cranes or hoists to prevent damage to the unit.

6.2.2 Inspection

On receipt of the equipment, inspect it for visible damage such as dents and abrasions that may have occurred in transit. Inspect the logic modules for foreign matter that may have lodged in them during shipment. Any damage should be reported immediately to both the Carrier and Digital Equipment Corporation. Check the contents of the carton with the shipping document. Immediately report any omissions or incorrect parts to Digital Equipment Corporation. Figure 6-2 shows the necessary RH10 installation data.

6.2.3 Power Requirements

The RH10 is equipped with self-contained power supplies and a DEC Type 857 Power Control. The +5 Vdc and +15 Vdc requirements of the unit are provided by DEC Type 742 Power Supplies. The -15 Vdc requirement is provided by a DEC Type 783 Power Supply.

6.2.4 RS04 Add-On Installation Procedure

This paragraph provides Field Service with the proper installation procedure for the RS04 disk unit added to PDP-10 systems. If the installation is not a field add-on, this procedure may be used as a check list to validate the originally configured subsystem. The following steps outline the procedure for unpacking, inspecting, and mounting the drive.

1. Open the RS04 shipping container and examine the drive for shipping damage.

2. Remove the disk from the container and place it on a flat surface with the top surface up. The RS04 is designed to be slide mounted in a standard DEC 19-in. rack, containing an 861 Power Control and cabinet stabilizers.

3. Remove the rack slide sections from the side of the disk by sliding them completely forward. Do not unscrew the slide sections which are mounted to the disk cabinet sides.

4. Refer to the RS04 configuration drawings located in the RH10 print set.

5. Insert the snap-on 10-32 Tinnerman nuts (90-07786) into the proper hole positions as indicated on the configuration drawing by "A" numbers and attach the rack slides.

   Upper drive – Holes 72, 75 from bottom.
   Bottom drive – Holes 44, 47 from bottom.

NOTE

DO NOT attempt to lift the RS04 by yourself. Two persons are needed.

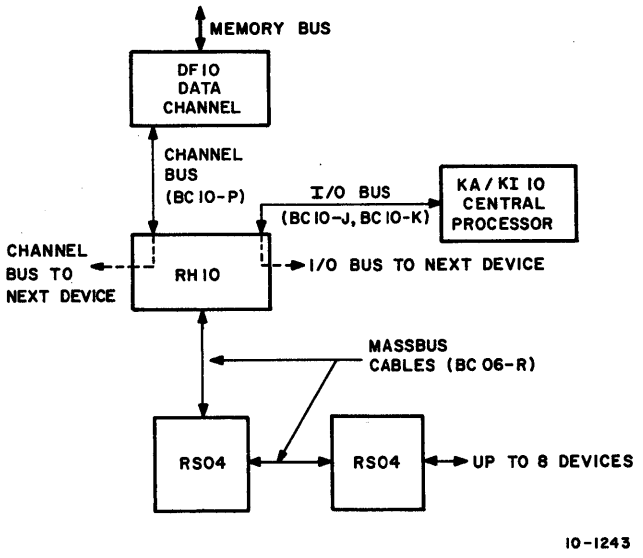


Figure 6-1 RH10/DF10/RS04 Cable Interconnection Diagram

6. Pick up the RS04 and slide it into the chassis slides just mounted. Slide the unit fully to the rear, making sure that all slides seat properly and interlock.

7. Extend the unit to its full out position on the slides. A lock click should be heard when the unit is fully extended.

NOTE

DO NOT APPLY POWER to the unit. The motor lock must be removed before power is applied.

8. Motor Lock

   a. After repeating step 7 above, remove the bottom chassis cover.

   b. Remove the motor lock, turn it 180° around, and secure it back into position with the brushes around the spindle shaft. The metal protection plate should be covering the brushes so that the brushes cannot be seen when viewing from the bottom.

9. Massbus Cable Connections

   a. Steps 8 and 9 must be completed before connecting cables. Refer to the RS04 Massbus cabling diagram in the RH10 print set.

   b. Remove the two Massbus cable restraints from the lower right rear corner of the drive.

   c. Route the three incoming Massbus ribbon cables marked Massbus A, B, and C through the right (viewed from the rear of the unit) cable clamp to the M5903 module area.

   d. Connect each cable to the proper module via the 3M connectors. Use the following table to locate the correct transceiver board.

Module	Slot	Cable
M5903	AB01	Massbus A
M5903	AB02	Massbus B
M5903	AB03	Massbus C

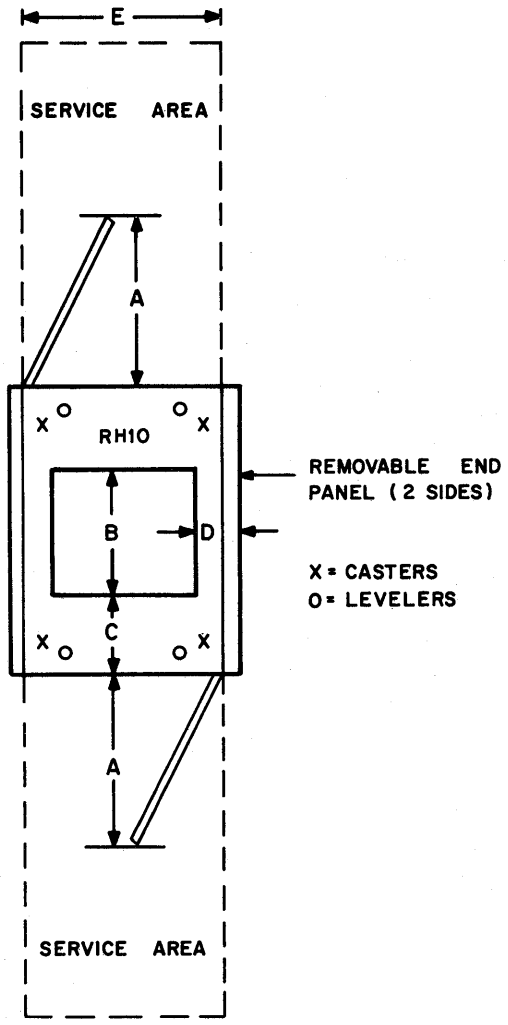
   e. If there are no more drives to be added to the Massbus, the bus must be terminated here. Insert three H870 Miniterminators into the remaining 3M cable connectors, one per M5903 module. (Some systems may contain an M5903YA module as a combined terminator and transceiver for the last drive on the Massbus.)

   f. If another drive is to follow, insert three output cables as in step c and dress them out through the rear of the drive via the left cable clamp (viewed from the rear).

   g. Secure both cable clamps and replace both covers. Slide the drive into the rack.

10. Power

   a. Insert the RS04 power plug into the unswitched side of the 861 Power Control.



DIMENSIONS	A	B	C	D	E	F
INCHES	20	15	7.5	3.2	20.5	36
METERS	.50	.38	.19	.08	.52	.91

10-1244

Voltage	Current @ 115 Vac	Power/Heat Dissipation	Dimensions			Weight	Operating Temperature	Storage Temperature	Relative Humidity	Max. Cable Length			Air Volume Inlet
			Height	Width	Depth					I/O	Channel	Massbus	
See Notes 1 and 2	5 13A Surge	570 W 1900 Btu/hr	72 in. 1.83 m	22 in. .56 m	30 in. .76 m	507 lbs 230 kg	60° to 90° F 15° to 35° C	40° to 110° F 5° to 45° C	20% to 80%	150 ft 45 m	100 ft 30 m	120 ft 36 m	800 ft^3/min 380 l/S (Top)

Note 1: 60 Hz Systems – This device requires an input of 115 V ± 10%, 60 Hz ± 2%, single-phase, 2-wire plus ground and is supplied with 25 ft (7.5 m) of 3 conductor wire and a Hubbell #3331 cord cap (male plug) which mates with a Hubbell #3330 receptacle. A 30 A circuit is recommended for this type of service.

Note 2: 50 Hz Systems – This device requires an input of 230 V ± 10%, 50 Hz ± 2%, single-phase, 2-wire plus ground and is supplied with a 3-terminal pressure connector block, 25 ft (7.5 m) of 3-conductor wire, and a Hubbell #3321 cord cap (male plug) which mates with a Hubbell #3320 receptacle. During equipment installation, this cord or cap may be removed and replaced with another cord or cap. A 15 A circuit is recommended for this type of service.

Figure 6-2 RH10 Installation Data

b. Connect the incoming remote power cable (3-wire) into J1 of the drive and output remote cable into J2, if applicable.

c. Connect the power sequence jumper into J3 if this is the first drive; otherwise, connect the incoming 4-wire power sequence cable to J3.

d. If this is the last drive or the only drive, no connection is made to J4. Otherwise, a 4-wire sequence cable is output from J4 to J3 of the next drive. Part numbers:

J1, J2 Cable, 3-wire	70-08288
J3 Jumper Plug, 1st device	70-09490
J3, J4 Cable, 4-wire	70-09491

e. Turn SW1 to "REMOTE" and the circuit breaker on. When the CPU is turned on, all drives (if multidrive) will power sequence up, one at a time.

f. The RS04 is now physically mounted. Refer to the RH10/RS04 Customer Acceptance Procedures located in the RH10 Print Set for on site acceptance procedures.

6.3 DIAGNOSTICS

The following three diagnostic programs are available with the RH10 subsystem.

MAINDEC-10-DCRHA	PDP-10/RH10 Deviceless Diagnostic
MAINDEC-10-DCRSA	PDP-10/RH10/RS04 Disk Static and Maintenance Diagnostic
MAINDEC-10-DCRSB	PDP-10/RH10/RS04 Disk Transfer and Reliability Diagnostic

6.3.1 Deviceless Diagnostic (DCRHA)

This diagnostic exercises the major portion of the RH10 with no Massbus device connected in the system. By using the RH10 maintenance panel, read and write data transfers can be simulated and the CPU memory to DF10, to RH10 Controller data path, is thoroughly tested without using the Massbus.

6.3.2 Static and Maintenance Diagnostic (DCRSA)

This diagnostic provides the majority of the testing for the RS04 without an actual disk surface being connected to the RS04. By utilizing the Maintenance mode feature of the RS04, read and write data transfers can be simulated and the CPU memory to DF10, to the RH10 Controller, to RS04 Disk Data Path, is thoroughly tested without using the RS04 disk surface (analog circuitry).

6.3.3 Disk Transfer and Reliability Diagnostic (DCRSB)

This diagnostic is an on-line reliability test for PDP-10 systems, consisting of a DF10 Data Channel and up to 8 disks. The operator can execute tests ranging from basic read or write operations up to complete diagnostic and reliability sequences. The program, which runs in EXEC mode only, loads with DDT providing extensive operator/program communication.

6.4 RH10 MAINTENANCE PANEL

The RH10 contains a maintenance panel and an indicator panel. The maintenance panel allows a means of exercising the RH10, the drive, and the Massbus, under local control. The indicator panel provides a visual indication of pertinent signals in the RH10 subsystem. Paragraph 6.4.1 provides a description of each of the switches on the maintenance panel and Paragraph 6.4.2 describes each of the indicators on the panel.

6.4.1 Maintenance Panel Switches

The maintenance panel consists of 12 thumbwheel switches and assorted toggle and pushbutton switches (Figure 6-3). With the LOCAL/REMOTE switch in REMOTE, the RH10 operates normally in conjunction with the DF10, the PDP-10 processor, and the associated drives. The maintenance panel is effectively disabled. With the LOCAL/REMOTE switch in LOCAL, the REG SEL and REG DATA thumbwheel switches are gated to the logic and appear as inputs from the I/O bus. Pressing the START button, generates the equivalent of DATAO CLEAR and DATAO SET pulses. Consequently, all DATAO instructions may be simulated by the maintenance panel. A brief description of each switch follows.

REG SEL Thumbwheel Switches – The REG SEL switches are two octal thumbwheel switches used to select the appropriate register. An octal 40_8 or greater set in these switches designates an RH10 register selected and an octal 37 or less set in these switches designates a drive register.

REG DATA Thumbwheel Switches – The REG DATA switches are 12 octal thumbwheel switches used to load 30 bits of data into the RH10 from the maintenance panel.

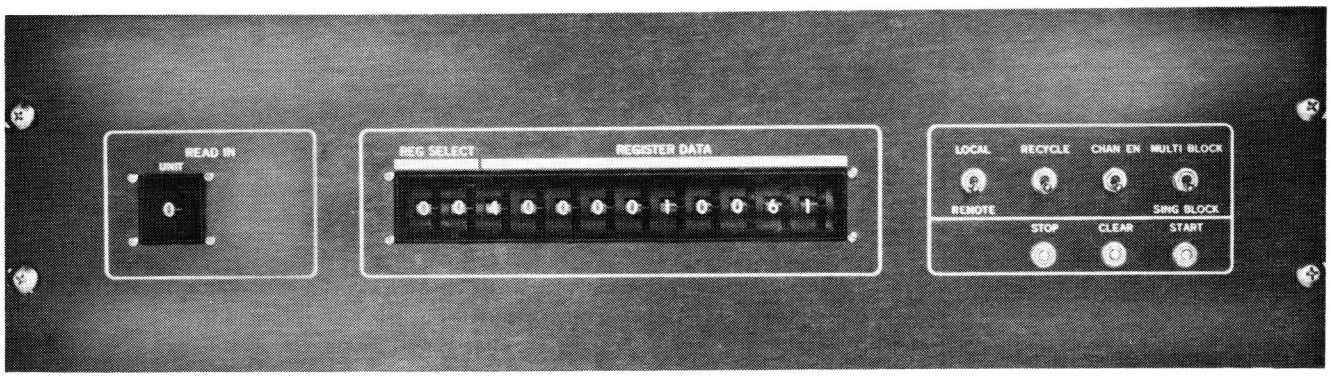


Figure 6-3 RH10 Switch Panel

LOCAL/REMOTE Toggle Switch – In LOCAL position, the maintenance panel is enabled to allow the operator to manually operate the system from the panel. In REMOTE position, all the maintenance panel switches are disabled, and the subsystem operates normally with the maintenance panel logically disconnected from the system.

NOTE

When the LOCAL/REMOTE switch is in LOCAL and is set to REMOTE, the RH10 is still in LOCAL MODE. The CLEAR pushbutton must be depressed to return the RH10 to REMOTE mode.

RECYCLE Toggle Switch – The RECYCLE switch allows the specific operation selected at the panel to be recycled. If the RECYCLE switch is OFF, the operation will be performed only once.

CHAN EN Toggle Switch – The Channel Enable (CHAN EN) switch logically connects the DF10 to the RH10 to allow communication between the two devices. If this switch is OFF, the two devices are logically disconnected.

SINGLE BLOCK/MULTIBLOCK Toggle Switch – If the SINGLE BLOCK/MULTIBLOCK switch is in SINGLE BLOCK position, the transfer will be for one block of data. If the switch is in the MULTIBLOCK position, the data transfer will be to the end of the drive (last track and last block).

START Pushbutton – Initiates DATAO SET and DATAO CLEAR pulses to allow the DATAO, selected by the maintenance panel, to be executed.

CLEAR Pushbutton – Clears all status indicators and registers. (Generates IBC PWR CLR).

STOP Pushbutton – When the RECYCLE switch is in the OFF position, this switch is rendered ineffective. When RECYCLE is ON, the STOP pushbutton terminates the recycling operation, if depressed.

6.4.2 Indicator Panel

The RH10 indicator panel is shown in Figure 6-4. Table 6-1 provides a brief description of the various indicators on the panel when they are illuminated. The indicator panel contains four rows of indicators which are generally divided as follows:

Top row – contents of Channel Buffer

Second row – channel control indicators and data buffer indicators

Third row – CR register indicators

Bottom row – Massbus indicators, error indicators, interrupt status, and priority interrupt assignment.

Where possible, the indicators are aligned vertically as a further memory aid. For example, the MAINT MODE indicator is bit 11 and the GEN EVC bit is bit 18, which are aligned under these respective bit positions.

Table 6-1
RH10 Indicator Panel

Name	Function
CHANNEL BUFFER 0–35	Displays the 36-bit data word from the DF10 during a write operation and displays the 36-bit data word read from the disk during a read operation.
CHAN CONT (Channel Control)	Denotes the DF10 Channel Control indicators.
ACT BUF (Active Buffer)	Indicates that a DATAO 40_8 instruction has been issued and the RH10 has requested the Data Channel (DF10) but has not obtained it.
CHAN ACT (Channel Active)	Indicates that a DATAO 40_8 instruction has been issued; the RH10 has requested the channel and has obtained it.
CHAN PLS (Channel Pulse)	Indicates that the DF10 has transmitted a Channel Pulse accompanying data for a write operation or indicates that the DF10 is ready to receive data for a read operation.
CHAN STRT (Channel Start)	Indicates that the RH10 is requesting a channel transfer with the DF10.
INH (Inhibit)	Indicates that the DF10 has been shut down by the RH10.
GEN CLR	Indicates that the DF10 Data Channel has been cleared.
CONT EXC (Controller Exception)	Indicates that the RH10 has raised the Exception Line which shuts down the drive.
FIN EN (Finish Enable)	Indicates that the RH10 and the drive have shut down.
RUN	Indicates that the RH10 has asserted the RUN line on the Massbus. This indicator stays on for the whole sector.
AR SYNC (Assembly Register Sync)	Indicates that the AR was empty for a write operation and that the AR was full for a read operation. Either condition may cause an overrun situation.
ODD BYTE	Indicates that an odd byte is present during a Read or Write. Set on the leading edge of SCLK.
EVEN BYTE	Indicates that an even byte is present during a write function. Set on the trailing edge of SCLK. EVEN BYTE is not used in a read operation.
CB FULL (Channel Buffer Full)	Indicates that the Channel Buffer has been loaded with a data word.
AR FULL (Assembly Register Full)	Indicates that the AR has been loaded with a data word.
DPA (Data Parity)	Indicates that a parity bit has been received from the drive.

Table 6-1 (Cont)
RH10 Indicator Panel

Name	Function
DATA BUFFER 0–17	Displays the data read from the disk during a read operation and displays the data read from the DF10 during a write operation.
CR REG SEL 0–3 (CR Register Select)	Displays the register address specified in the last DATAO 40_8 instruction issued to the RH10. For example, if a DATAO 40 was the last instruction, bit 0 would be lit and the others would be off.
CR CBTO (Control Bus Timeout)	Displays a control bus timeout when the RH10 tries to write a data transfer function code and the GO bit in the drive and receives no response from the drive.
DBTO (Data Bus Timeout)	Displays a data bus timeout when the RH10 issues a read or write command and receives no response from the drive.
MAINT MODE (Maintenance Mode)	Used for diagnostic programming. Indicates the RH10 is disconnected from the Massbus device and the RH10 can only be single-stepped by issuing DATAO 50 instructions. The clocks and data (read operation) from the drive are simulated by the programmer.
CR DR SEL 0–2 (Drive Select)	Represents the address of the drive that the RH10 is to perform a read or write operation on when during a DATAO 40_8 instruction.
GEN EVD (Generate Even Parity–Data Bus)	Indicates that even parity is generated on the data bus. Used by the diagnostic programmer to check drive parity network for a write operation and to check the RH10 parity network during a read operation.
DXES (Disable Transfer Error Stop)	Indicates that drive exception, channel data parity error and data bus parity errors are disabled from shutting down the RH10. The DXES bit is used in software error recovery routines.
INIT CW ADDR 27–34 (Initial Control Word Address)	Displays the initial starting command list address in the DF10. Loaded with the DATAO 40_8 instruction.
WTEM (Write Even Parity Memory)	Indicates that data written into core during a read operation will be written with even parity. This feature is used by diagnostic programmer to check the parity network. Loaded with the DATAO 40_8 instruction.
CR FUNC CODE 0–4 (Control Register Function Code)	Displays an RH10 read or write operation. Bits 0, 1, 2 and GO bit specify a read operation (71_8); bits 0 and 1 and GO bit specify a write operation (61_8). Loaded by the DATAO 40_8 instruction.
GO	Loaded by the DATAO 40_8 instruction. Indicates that the drive is connected to the Controller and has been addressed to do a transfer.
DIB REG SEL 0–4 (DIB Register Select)	Indicates the drive register selected, for a DATAO/I 00–37_8, i.e., a DIB cycle.

Table 6-1 (Cont)
RH10 Indicator Panel

Name	Function
CTOD (Controller to Drive)	Indicates the direction of transfer. The indicator is ON for a Controller-to-drive transfer and OFF for a drive-to-Controller transfer.
DIB CBTO (Control Bus Timeout)	Indicates a Timeout has occurred on the control bus for a DIB cycle.
CBPE (Control Bus Parity Error)	Indicates a parity error has been detected in the RH10 when reading a drive register.
DATA LATE	Indicates that a DATAI instruction was issued to read to the DIB register while a DIB cycle was in progress.
ILL COM (Illegal Command)	Indicates that an attempt was made to write the drive's control register with a read or write function code when doing a DIB cycle.
DIR DR SEL 0–2 (Drive Select)	Indicates the drive selected for a DIB cycle.
GEN EVC (Generate Even Parity Control Bus)	Indicates that even parity is being generated while writing a drive register and checks the drive's parity checking network. Also checks RH10 parity network on a read operation.
CPA (Control Parity)	Stores the state of the control bus parity line from the last drive register read.
DIB REG DATA 0–15	Stores the data read from a drive when reading a drive register or stores the data to be written into a drive register when doing a write operation.
RAE 0–7 (Register Access Error)	One RAE error indicator (0–7) is associated with each drive. The Register Access Errors are CBTO, CBPE, DATA LATE and ILL COM.
READ-IN	Indicates that the RH10 is being set to READ-IN mode from the CPU console.
LOCL STOP (Local Stop)	LOCL STOP indicator must be ON for the RH10 to be in LOCAL mode. LOCL STOP is normally ON but may be put ON by the CLEAR pushbutton on the maintenance switch panel.
LOCL (Local)	Indicates that the RH10 is in LOCAL mode and is operating from the maintenance switch panel.
KI INTR	Indicates that the Interrupt Address Register is enabled to allow the program to interrupt to an address. This is set up by the programmer.
MSBC (Massbus Control)	Denotes the Massbus control indicators.

Table 6-1 (Cont)
RH10 Indicator Panel

Name	Function
DIB REQ (DIB Request)	Indicates a DATAO $00_8 - 37_8$ instruction has been received by the RH10.
CONT REQ (Control Request)	Indicates that a DATAO 40_8 has been received by the RH10.
DIB CYC (DIB Cycle)	Indicates that the last cycle or the cycle in progress is a DIB cycle.
CYC ACT (Cycle Active)	Indicates that a Massbus cycle is in progress.
DEM (Demand)	Indicates that the DEM signal is asserted on the Massbus by the RH10.
ERROR STATUS	Denotes status of error conditions.
DBPE (Data Bus Parity Error)	Indicates that a parity error is present on the data bus during a read operation.
DR EXC (Drive Exception)	Indicates that the drive has raised the Exception line due to an error condition.
CDPE (Channel Data Parity Error)	Indicates that the DF10 has fetched a data word and flagged a parity error on the memory bus. This condition causes the DF10 to send a pulse to an error flip-flop in the RH10 forcing the CDPE indicator to go ON.
CWPE (Control Word Parity Error)	Indicates that the DF10 has fetched a control word and flagged a control parity error on the memory bus. This condition causes the DF10 to send a pulse to an error flip-flop in the RH10 forcing the CDPE indicator to go ON.
NXM (Non-existent Memory)	Indicates that the DF10 did not get a memory response within 100 μs.
OVERRUN	Indicates that the disk is overrunning the RH10 during a read operation (no place to unload the data) or that the data was not available to the disk during a write operation.
ILFC (Illegal Function Code)	Indicates that a DATAO 40_8 instruction with some function code other than a read or write code has been specified.
SD RAE (Selected Drive Register Access Error)	Indicates that a DATAO 40_8 has been issued to a drive which has a Register Access Error condition previously detected. The data transfer is inhibited, the operation is aborted, and the SD RAE indicator goes ON.

Table 6-1 (Cont)
RH10 Indicator Panel

Name	Function
CW WRT (Control Word Write)	Indicates that the DF10 has written a control word in response to a Control Word Request (specified by a CONO instruction with bit 26 asserted).
PS FAIL (Power Supply Fail)	Indicates that a low voltage condition has been detected in the RH10 power supplies.
INTR STATUS (Interrupt Status)	Denotes the conditions generating program interrupts.
CBOV (Control Bus Overrun)	Indicates that a DATAO $00–37_8$ instruction has been issued to the DIB register when a DIB cycle was already in progress.
RAE (Register Access Error)	Indicates a register access error in a drive. This indicator represents the OR condition of the 8 RAE indicators (RAE 0–7).
ATTN (Attention)	Indicates that a drive has raised the Attention Line on the Massbus. This indicator represents the OR condition of all the drive attention lines.
BUSY	Indicates that the RH10 is doing a data transfer. BUSY does not raise an interrupt.
DONE	Indicates completion of a data transfer to the CPU.
PIA 33–35	Represents the address of the interrupt channel that will cause a program interrupt.

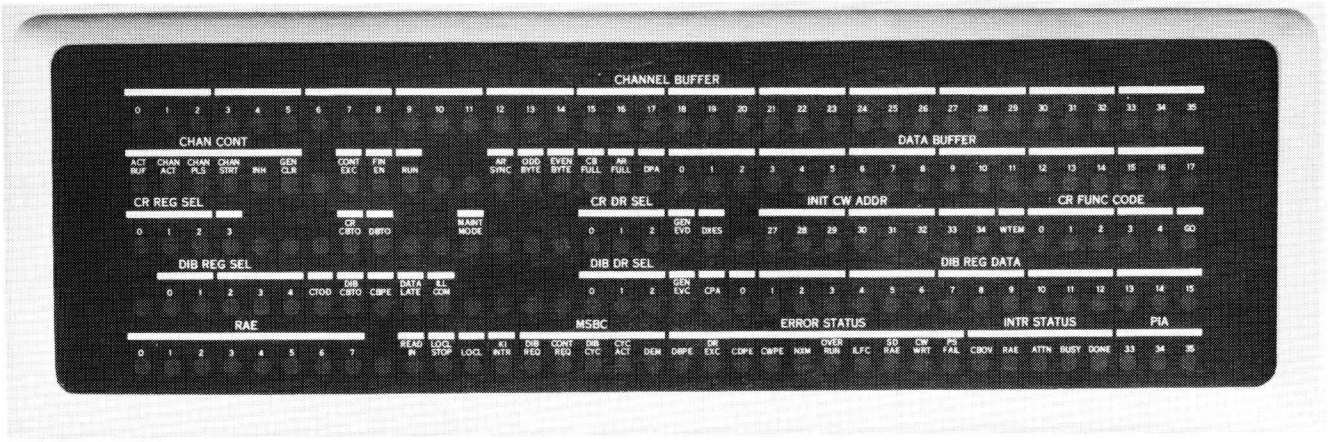


Figure 6-4 RH10 Indicator Panel

6.5 USES OF MAINTENANCE PANEL

The RH10 maintenance panel can (1) exercise the RH10 only, (2) can exercise the RH10 with a drive, (3) can exercise the RH10 with the DF10 and simulate a drive, or (4) can exercise the entire system including the memory, DF10, RH10, and the associated drive. Examples of each of these operations is provided in the following paragraphs:

EXAMPLE 1 – Exercise RH10 only

Operation to be performed: Issue a DATAO 40_8 to the RH10 Control register to select drive number 7.

a. Place LOCAL/REMOTE switch to LOCAL.

b. Place RECYCLE switch OFF.

c. Place CHAN EN switch OFF.

d. Place SINGLE BLOCK/MULTIBLOCK switch to SINGLE BLOCK.

e. Deposit 40_8 in REG SEL thumbwheel switches. These switches represent bits 0–5 of the DATAO instruction. The 40_8 specifies a DATAO to the RH10 Control register.

f. Deposit 4007 000000 in the REG DATA thumbwheel switches. The four octal digits on the left represent bits 6–17 of the instruction and the 6 octal digits on the right represent bits 18–35. The switches are set to the Control register format (40_8 as shown in Chapter 3). Note that bit 6 is the Load register bit which is a 1 and yields the octal 4 in this example. Bits 15–17 are the drive select bits which are all 1's to select drive number 7.

g. Depress STOP pushbutton.

h. Depress CLEAR pushbutton.

i. Depress START pushbutton.

j. Examine CR DR SEL indicators on the RH10 indicator panel. All three should be illuminated, indicating drive number 7 is selected.

NOTE

All RH10 registers can be tested in this manner except for bit 35 of the CR register. This bit signifies the start of a data transfer.

EXAMPLE 2 – Exercise RH10 Connected to a Drive

Operation to be performed: write and read 1's on all sectors and tracks of the disk.

a. Depress the CLEAR pushbutton. This will clear the DA register in the drive.

b. Place the SINGLE BLOCK/MULTIBLOCK switch to the SINGLE BLOCK position.

c. Set the REG SEL thumbwheel switches to 50_8 (DATAO to RH10 data buffer).

d. Set the REG DATA thumbwheel switches to 4000 777777.

e. Depress the START pushbutton. All 1's should now be loaded into the data buffer.

NOTE

Do not depress the CLEAR pushbutton.

f. Set the REG SEL thumbwheel switches to 40_8 (DATAO to RH10 Control register).

g. Set the REG DATA thumbwheel switches to 4000 000061 (DATAO RH10 Control register, write function code, drive no. 0).

h. Depress the START pushbutton. This will write all 1's on the entire disk. The data transfer will terminate with a DRIVE EXCEPTION error. This is normal termination.

i. Depress STOP pushbutton.

j. Depress the CLEAR pushbutton. This clears the DA register in the drive.

k. Set the REG SEL thumbwheel switch to 40_8.

l. Set the REG DATA thumbwheel switches to 4000 000071 (DATAO RH10 Control register, read function code, drive no. 0).

m. Depress the START pushbutton. This will read all sectors and tracks of disk no. 0. The transfer will terminate with a DRIVE EXCEPTION error. This is the normal termination and no other error conditions should be evident.

The data patterns can be changed by loading various data patterns in the data buffer prior to doing the write. The data written will be verified by the drive performing a CRC check after each sector read. If a read error occurred, it can be verified by visually checking the error LED's in the RS04 module rack after completion of the transfer. Scope loops can be attained by turning the RECYCLE switch ON prior to executing the read or write commands to the RH10 Control register.

NOTE

If it is desired to write or read a particular sector of the disk, place the SINGLE BLOCK/MULTIBLOCK switch to the SINGLE BLOCK position, prior to loading the RH10 Control register with the read/write function code. Load the DA register in the drive with the desired sector and track. If a scope loop is desired, make sure that the CLEAR push-button is not depressed prior to issuing the DATAO 40_8. This will allow the desired address data to remain in the DIB register and an automatic reload will occur at the end of each read or write cycle if the RECYCLE toggle switch is ON.

EXAMPLE 3 – RH10 Connected to PDP-10, DF10, and Memory

Operation to be performed: Write 1's into memory.

a. Deposit 000000 000200 in address 100 (Initial Control Word Address) in core memory. This is a jump to location 200.

b. In memory address 101, load all 0's. This will eventually be loaded with the termination word.

c. In memory address 200, load 777776 000277. This indicates a two-word transfer is to be accomplished, starting at location 277 + 1 or 300.

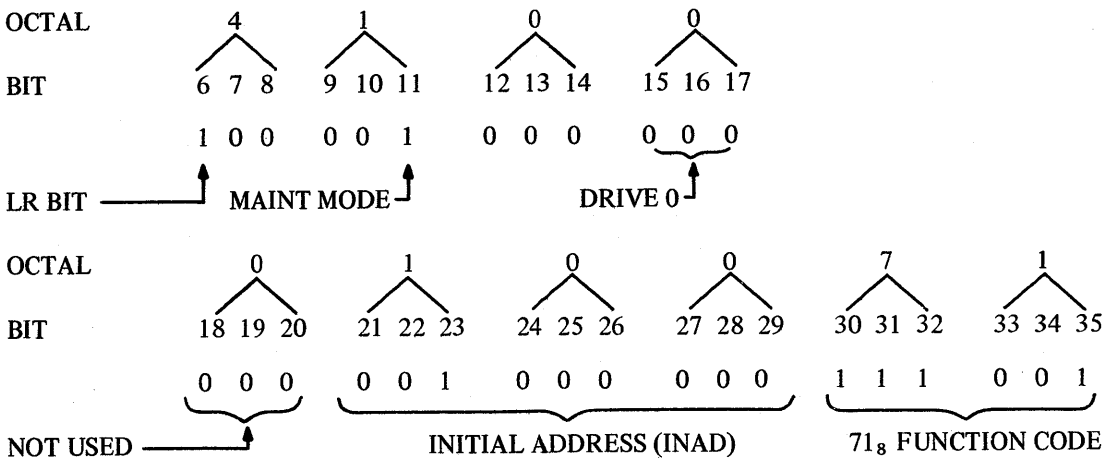
d. In memory address 201 load all 0's. This will subsequently contain the control word address plus 1.

e. In memory addresses 300 and 301, load all 0's. These memory locations will contain the data which is to be transferred from the RH10.

f. On the RH10 maintenance panel, set the RECYCLE switch OFF, the CHAN EN switch ON, the SINGLE BLOCK/MULTIBLOCK switch to SINGLE BLOCK and the LOCAL/REMOTE switch to LOCAL.

g. Set the REG SEL thumbwheel switches to 40 (DATAO to RH10 Control register).

h. Set the REG DATA thumbwheel switches to 4100 010071. These bits are decoded as shown below:



The MAINT MODE bit, being asserted, allows the RH10 to simulate SCLK signals, since the drive is not connected. The 71_8 function code specifies a read data transfer.

i. Depress the STOP pushbutton.

j. Depress the CLEAR pushbutton.

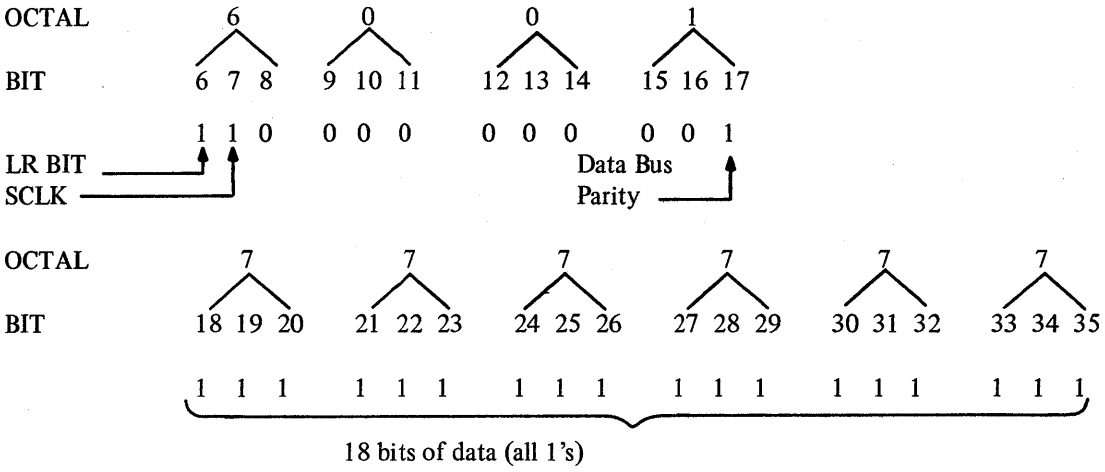
k. Depress the START pushbutton.

l. Set the REG SEL thumbwheel switches to 50 (DATAO to the data buffer).

m. Set the REG DATA thumbwheel switches to

6001 777777

This is decoded as follows:



NOTE
Do NOT depress the STOP or CLEAR pushbuttons.

n. Depress the START pushbutton THREE times. Depressing the switch twice loads memory address 300 with all 1's. The third switch depression assembles another 18 bits in the data buffer in the RH10. This word is then transferred to the AR.

o. Set the REG DATA thumbwheel switches to

7001 777777.

The addition of bit 8 on a 1 will cause an EBL pulse on the next START.

NOTE
Do NOT depress the STOP and CLEAR pushbuttons.

p. Depress the START pushbutton. This reads the 18 bits from the REG DATA switches. These bits are strobed in the DB and are then combined with the 18 bits already stored in the RH10 and the complete 36-bit word is transferred to memory address 301.

q. Examine memory location 300 and 301 by depressing the EXAMINE switch on the PDP-10 console. The contents of location 300 and 301 should be all 1's.

r. Examine address 101. This location should contain the termination word which is

000201 000301, where

201 = control word address +1, and

301 = last data word address referenced by the DF10.

EXAMPLE 4 – RH10/DF10/Memory/RS04 and PDP-10 Processor Connected as System

Operation to be performed: (1) Write 1's into the RS04 on sector 11, track 11. (2) Then, read 1's from sector 11, track 11 for transfer to memory.

a. Deposit 000000 000200 in memory address 100 (initial address). This is a jump to location 200.

b. Deposit all 0's in memory address 101. This address will contain the termination word.

c. Deposit 777770 000277 in memory address 200. The left-half denotes a two's complement transfer of seven words to the location specified in the right-half, which is memory address 277 + 1 or 300.

d. Deposit all 1's in memory addresses 300–307.

e. On the RH10 maintenance panel, set the RECYCLE switch OFF, the CHAN EN switch ON, the SINGLE BLOCK/MULTIBLOCK switch to SINGLE BLOCK, and the LOCAL/REMOTE switch to LOCAL.

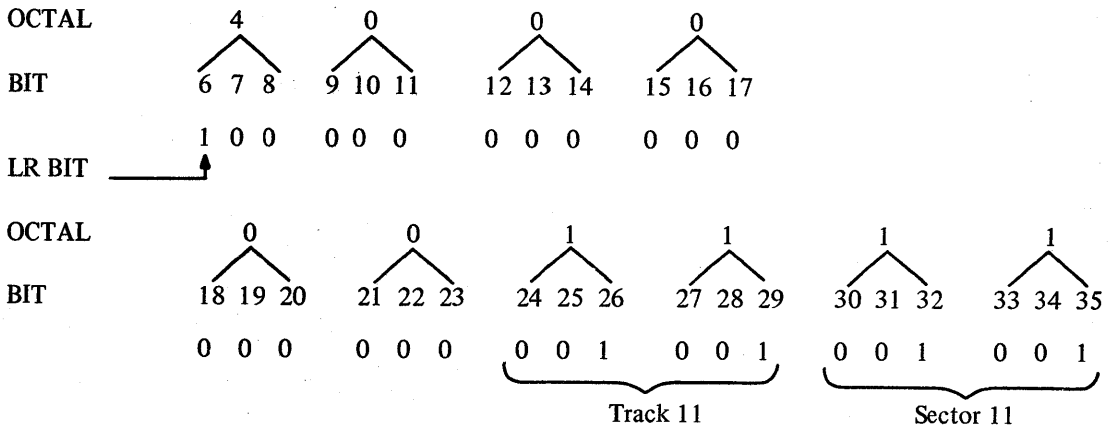
f. Make sure the RS04 is powered up and properly cabled to the RH10.

g. Set the REG SEL thumbwheel switches to 05_8 (DATAO to Desired Address Register in the Drive).

h. Set the REG DATA thumbwheel switches to

4000 001111

This is decoded as follows:



i. Depress the STOP pushbutton.

j. Depress the CLEAR pushbutton.

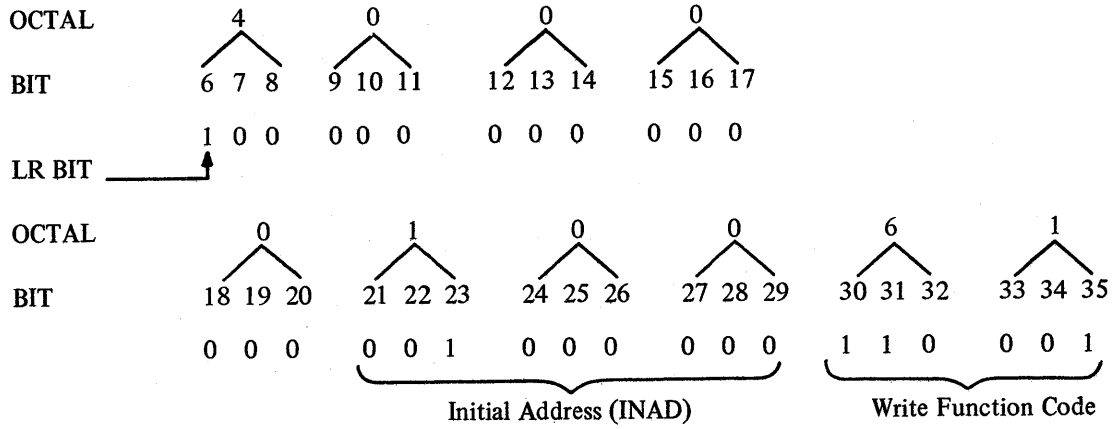
k. Depress the START pushbutton.

l. Set the REG SEL thumbwheel switches to 40_8 (DATAO to RH10 Control register).

m. Set the REG DATA thumbwheel switches to

4000 010061

This is decoded as follows:



NOTE
Do NOT depress the STOP or CLEAR pushbuttons.

n. Depress the START pushbutton. This writes seven words containing all 1's into sector 11, track 11.

o. Examine memory address 101. This location should contain the following termination word:

000201 000307, where

201 is the control word address + 1 and the 307 is the last address referenced by the DF10.

NOTE
If this is not correct, there is a malfunction in the memory, DF10, RH10, or RS04, and a subsequent read back of this data will be in error.

p. Loads 0's into memory addresses 300–307. This ensures that when we read 1's from the disk that all 1's were really transferred.

q. Set the REG SEL thumbwheel switches to

4000 001111

This causes the RS04 to read from the same sector and track that was just written (sector 11, track 11).

r. Depress the STOP pushbutton.

s. Depress the CLEAR pushbutton.

t. Depress the START pushbutton.

u. Set the REG SEL thumbwheel switches to 40_8 (DATAO to RH10 Control register).

v. Set the REG DATA switches to

4000 010071

This specifies a read data transfer with an initial memory address of 100.

NOTE
Do NOT depress the STOP or CLEAR pushbuttons.

w. Depress the START pushbutton. This causes seven words to be read from sector 11, track 11 of the disk into memory locations 300–307. To verify, examine these memory locations. They should contain all 1's.

x. Examine memory address 101 which should contain the termination word shown below

000201 000307, where

201 is the control word address plus 1 and the 307 is the last data word address referenced by the DF10.

By changing core memory, it is possible to read or write various bit patterns on the disk. Note that in doing a read from the disk, the data last stored on the disk is the data that is read. By changing the DF10 Command List, it is possible to use different initial addresses (INAD's). The number of block transfers can be increased by using the MULTIBLOCK switch setting which will cause transfers from the point of reference to the end of the disk. For scope looping, the RECYCLE switch can be employed which will cause the specified operation to be repeated. For example, if the SINGLE BLOCK/MULTIBLOCK switch is in MULTIBLOCK and the RECYCLE switch is on and a write or read from sector 6, track 6 is specified, the write or read would start at this point, sequence through the rest of the blocks until the end of the disk and recycle to sector 6, track 6, where the process would be repeated.

APPENDIX A
RP04 MOVING HEAD DISK DRIVE

A.1 GENERAL

In addition to controlling the RS04, the RH10 can also be used in systems containing the RP04 Moving Head Disk Drive. The interface to the Massbus is identical. The system designation for the combination of RH10 and RP04(s) is RHP04. All channel bus, I/O bus, and Massbus operations described for the RH10/RS04 in the *RH10 Maintenance Manual* apply to the RP04.

The RP04 has more Massbus registers (16) than the RS04 and more bits implemented in some of the previously existing registers. Figure A-1 shows formats for all RP04 Massbus registers. Detailed descriptions of these registers and of all RP04 operations are in the *RP04 Device Control Logic Maintenance Manual* (DEC-00-HRP4M-A-D). Table A-1 lists the Massbus commands.

Basically, the RP04 consists of a disk drive manufactured by Information Storage Systems Inc., and a Device Control Logic (DCL) box which attaches to the side of each drive. The DCL is the interface to the RH10 controller via the Massbus. All registers and interface logic are contained within the DCL.

The command codes in Table A-1 may be set in the last two octal digits of the switch panel. They are displayed in the CR FUNCTION CODE lights.

A.2 CONFIGURATION

The RP04 connects to the RH10 by means of a round Massbus cable assembly (BC06S). A 5-foot flat cable (BC06R) is used within the DCL from the round cable transition connector up to the M5903 standard Massbus transceiver modules in the DCL. Two round cable connection paths exist: one for input from the previous RH10 and one for output to the next device.

Table A-1
RP04 Commands

Octal Code	Command
01	NO OP
03	UNLOAD
05	SEEK
07	RECALIBRATE
11	DRIVE CLEAR
13	RELEASE
15	OFFSET
17	RETURN TO CENTERLINE
21	READ IN PRESET
23	PACK ACKNOWLEDGE
31	SEARCH
51*	WRITE CHECK DATA
53**	WRITE CHECK HEADER AND DATA
61	WRITE DATA
63	WRITE HEADER AND DATA
71	READ DATA
73	READ HEADER AND DATA

*Equivalent to Read Data (71)
**Equivalent to Read Header and Data (73)

The last drive in the system must be terminated with three M5903YA transceiver cards or three H870 terminator modules inserted into the M5903 header slots. A preferred method is to install a termination block (P/N 7009938) containing H870 modules on the final, round cable connector block.

NOTE

CB1 may be OFF in the terminating drive, i.e., no power applied, yet the Massbus will operate.

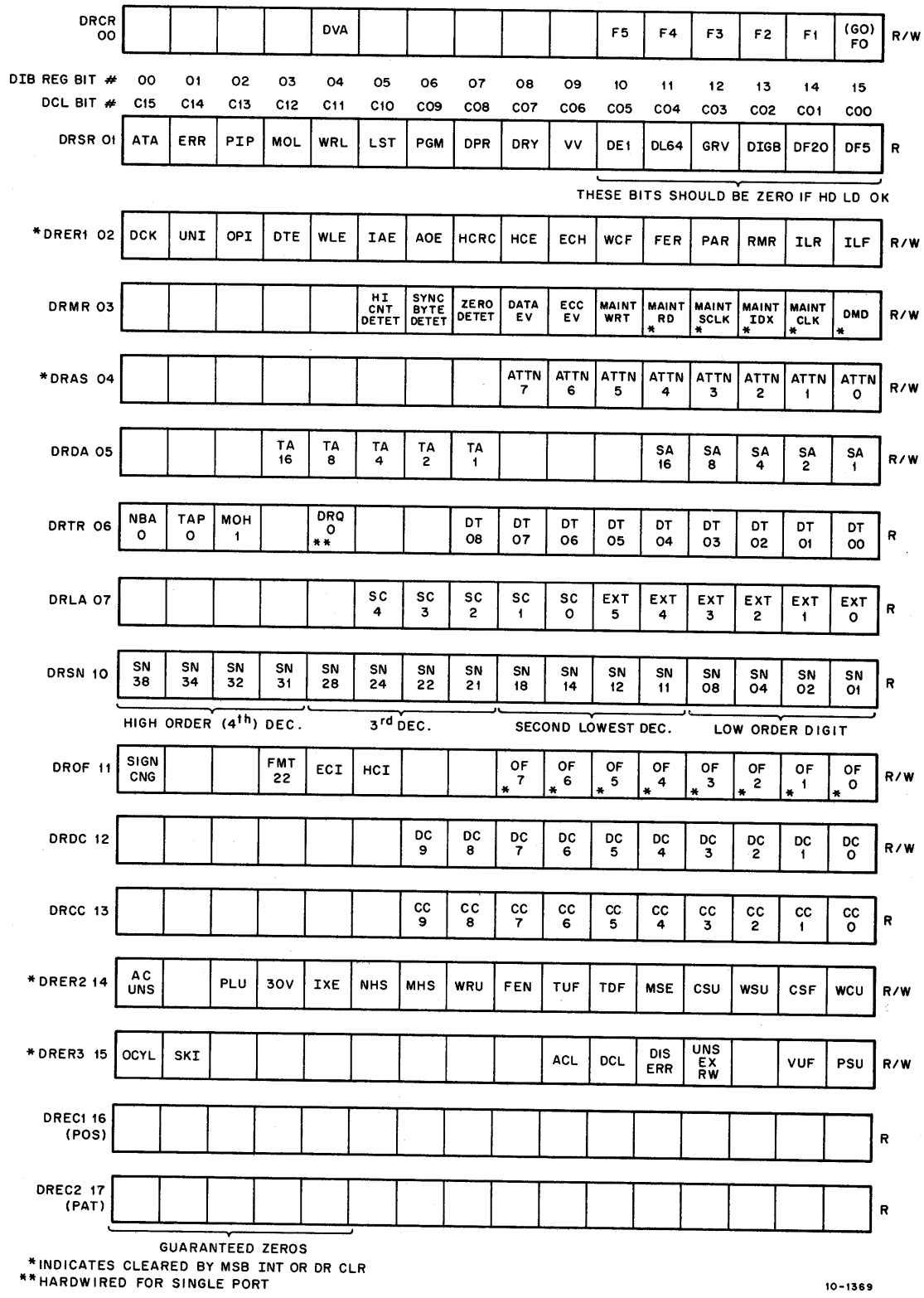


Figure A-1 RP04 Massbus Register Formats

With the round cable scheme, cables 2 feet in length connect from drive to drive in configurations containing up to 8 drives (max). The cable connecting the RH10 to the first drive can, therefore, be up to 40 feet long. The total length of 50 odd feet of round cable must not be exceeded.

Existing software does not support RP04s and RS04s on the same RH10.

A.3 INSTALLATION AND CHECKOUT

A.3.1 Installation

The following sequence must be followed when adding RP04 disk drives to the RH10:

a. Remove appropriate side panels from RP04s that are to be installed side by side.

b. Once the drive is in position, remove the read carriage locking mechanism from the drive shroud.

c. Refer to Chapter 2 of the *Model 733 DECdisk Storage Drive Operation, Service and Diagrams Manual* for drive installation procedures.

d. Connect the drives and controller using BC06S round Massbus cable assemblies. Terminate the last drive as described in Paragraph A.2.

e. Connect the RP04 to the power source [refer to Paragraph 1.3 of the *RP04 Disk Drive Installation Manual* (DEC-00-HRP41-A-D) for power requirements].

f. After completing the drive installation procedure, ensure that phasing is correct by noting that the pack spins in a counterclockwise direction. If not, reverse the phases in the power box.

g. Add skirts.

A.3.2 Diagnostic Descriptions

The following diagnostic programs are provided:

MAINDEC-10-DCRHA
PDP-10/RH10 Deviceless Diagnostic
MAINDEC-10-DCRPF
RP04 Disk Static and Maintenance Diagnostic
MAINDEC-10-DCRPG
RP04 Disk Transfer and Reliability Diagnostic

Each diagnostic is described in the following paragraphs.

A.3.2.1 Device Diagnostic (DCRHA) — This program exercises the major portion of RH10 logic; a Massbus device need not be connected to the system. The I/O bus and DF10/DF10C channel bus paths are thoroughly exercised.

A.3.2.2 Status and Maintenance Diagnostic (DCRPF) — This program exercises all RP04 Massbus registers and checks Massbus error conditions. Simple data transfers to and from the disk are executed. Basic mechanical movements are tested. The program can be caused to loop on errors.

This diagnostic is useful in isolating Massbus cable and transceiver problems during installation. It should also be run after replacement of any DCL board, before attempting more complicated programs.

A.3.2.3 Disk Transfer and Reliability Diagnostic (DCRPG) — This is an on-line reliability diagnostic program for RHP04 systems consisting of an RH10 with an associated DF10/DF10C data channel and up to 8 drives. Basic and complex data transfers and mechanical movements are executed, depending upon the test(s) selected.

A.3.3 Checkout

The following paragraphs provide system checkout procedures including examples for each procedure.

A.3.3.1 RH10 Maintenance Panel — The maintenance panel (Figure 6-3) is useful for off-line troubleshooting of an initial installation before running dedicated diagnostic programs. Most cable and DCL problems can be found and repaired in this manner, although MAINDEC-10-DCRPF resolves these problems also. Refer to Paragraphs 6.4 and 6.5 for a detailed description of the maintenance panel.

A.3.3.2 Off-Line Testing with the Maintenance Panel

Example 1 — Initial Hookup

a. Place the LOCAL/REMOTE switch in the LOCAL position. All other switches are OFF.

b. Start drive(s) and ascertain that the CONTROLLER SELECT switch points to the correct port. Wait for READY to come ON.

c. Deposit 01 000N 000000 in the switches. N is the number of the drive to be tested. Register 1 (DRSR) is read; this is the drive status register.

d. Press CLEAR, then press START.

e. The DIB register data should be 010600 (starting with bit 0 as the first and total octal digit). See Figure A-1. If the DIB register data is not correct, check the DIB CBTO light. If this is ON, the drive did not recognize the command. In any case, the cables and drives in the chain are suspect. If problems exist, power down the drives (CB1 OFF) to eliminate DCL faults and investigate cable/transceiver problems using one drive.

NOTE

The terminators do not require power to operate.

f. If the response was correct, deposit 00 400N 000021 in the switches. This is a read-in preset command.

g. Press CLEAR, then press START.

h. Repeat steps c. and d.

i. The DIB register data should be 010700. The Volume Valid bit is now set.

j. If this data is not correct, set the RECYCLE switch to ON and repeat steps f. and g. Dynamic logic problems can only be observed with the oscilloscope.

Example 2 — Read Data

a. Execute steps a. through d. of Example 1.

b. Deposit 40 400N 000071 (read data command) in the switches.

c. Press CLEAR, then press START.

d. The indicator panel should show DONE and FIN EN on; BUSY, DR EXC, DBTO, CBTO, and RUN should be off. DBTO indicates that the DCL failed to respond to the command. If DBTO is set, use Example 3 to set up an oscilloscope loop.

e. If DR EXC is set, proceed as follows.

f. Deposit 02 000N 000000 in the switch panel.

g. Press START; do not press CLEAR.

h. The contents of Error register 1 are now displayed. Analyze this data using Figure A-1. Repeat steps f. through h. using 14, then 15 as the first two digits (to read Error registers 2 and 3).

Example 3 — Recycle Read

a. Place the LOCAL/REMOTE switch in the LOCAL position. All other switches are OFF.

b. Deposit 00 400N 000021 in the switches.

c. Press CLEAR, then press START.

d. Deposit 01 000N 000000 in the switches.

e. Press START.

f. Check the DIB register data for 010700. Steps d., e., and f. are for continuity only.

g. Deposit 05 400N 000000 in the switches. This sets the track and sector address to zero. When recycling, this DIB command will be re-executed following every read.

h. Press START; do not press CLEAR.

i. Deposit 40 400N 000071 in the switches.

j. Set RECYCLE to ON and press START. The drive is now continually reading cylinder, track, sector 0, and can be examined with an oscilloscope. If the entire disk is to be read, omit steps g. and h. and the RH10 will automatically move through the entire disk.

Example 4 — Write Data

a. Place the LOCAL/REMOTE switch in the LOCAL position. All others are OFF.

b. Deposit 00 400N 000021 in the switches.

c. Press CLEAR, then START.

d. Deposit 40 400N 000061 in the switches.

e. Press START.

f. The indicator panel should show DONE and FIN EN on; DR EXC, DBTO, and RUN should be off. Debug, if necessary, using Examples 2 and 3 but using function code 61 (Write Data).

g. The data buffer indicators display data that was written onto the drive; zeros in this case.

h. To set a data pattern into the data buffer for writing, set the switches to 50 400N PPPPPP where P is the pattern.

i. Press START and repeat steps d. and e.

NOTE
Do not press CLEAR; this will erase the error.

Example 5 — Write Data Using the Channel

a. Deposit 000000 000200 in memory location 100 (initial address). This is a jump to location 200.

b. Deposit all 0s in location 101. This location will contain the termination word.

c. Deposit 777770 000277 in memory location 200. This control word will transfer 10 words to the RP04 from memory locations 300—307.

d. Deposit all 0s in location 201. This is the termination control word.

e. Load memory locations 300—307 with desired data pattern.

f. Set the switches to select LOCAL, CHAN EN, and SINGLE BLOCK. All others OFF.

g. Deposit 00 400N 000021 in the data switches.

h. Press CLEAR, and then START.

i. Deposit 40 400N 010061 in the switches. This is a write command with an INAD (initial control word address) of 100.

j. Press START. *Do not press STOP or CLEAR.* This will write the data pattern onto the drive at address zero. A different drive address can be selected by loading register 12 with the desired cylinder address and register 5 with the desired track and sector address before performing step h.

k. Examine memory location 101. This location should contain the termination word 000201 000307. The left half is the control word address +1; the right half is the last memory address referenced by the channel.

Example 6 — Read Data Using the Channel

a. Perform steps a., b., and c. in Example 5.

b. Deposit 0s into locations 300—307. Data read from the drive will be deposited in these locations.

c. Perform steps e., f., and g. in Example 5.

d. Deposit 40 400N 010071 in the switches. This is a read command with an INAD of 100.

e. Press START. *Do not press STOP or CLEAR.* This will cause ten words to be transferred from disk location 0 to memory locations 300—307.

f. Examine these locations to verify data.

g. Examine location 101. It should contain the termination word 000201 000307.

Example 7 — Seek Sequence

a. Set the LOCAL/REMOTE switches to LOCAL, all other switches to OFF.

b. Deposit 00 400N 000021 in the switches. Press CLEAR, then START.

c. Deposit 12 400N 00XXXX in the switches. Set switches to the desired cylinder address.

d. Press START. *Do not PRESS CLEAR.*

e. Deposit 05 400N 0XX0YY in the switches. Set switches to the desired track address and switches to the desired sector address.

f. Press START. *DO NOT PRESS CLEAR.*

g. Deposit 00 400N 000005 in the switches.

h. Press START.

A.3.3.3 DCRPF Initial Verification — MAINDEC-10-DCRPF is useful in verifying correct Massbus hookup as well as testing Massbus registers and performing basic data transfers. To verify Massbus operation, run MAINDEC-10-DRSTAT which uses the control bus only, checking the read/write capabilities of all DCL registers. If problems occur, isolate to the drive, then the module. Figure A-2 is a block diagram of the RP04 DCL. This diagram is useful for identifying defective modules flagged by MAINDEC-10-DRSTAT. For example, an inability to write DRER3 (15) would map to replacement of the EC board. If data showed parity errors while writing, the Massbus transceiver, the EC board MUX, or the SN board buffer and parity network would be suspect. If more than one drive is affected, power down all drives but one (CB1 OFF) and isolate the Massbus problem.

After running MAINDEC-10-DRSTAT, run data which verifies the data bus portion of the Massbus. Successful operation of these programs assures correct cabling and transceiver operation.

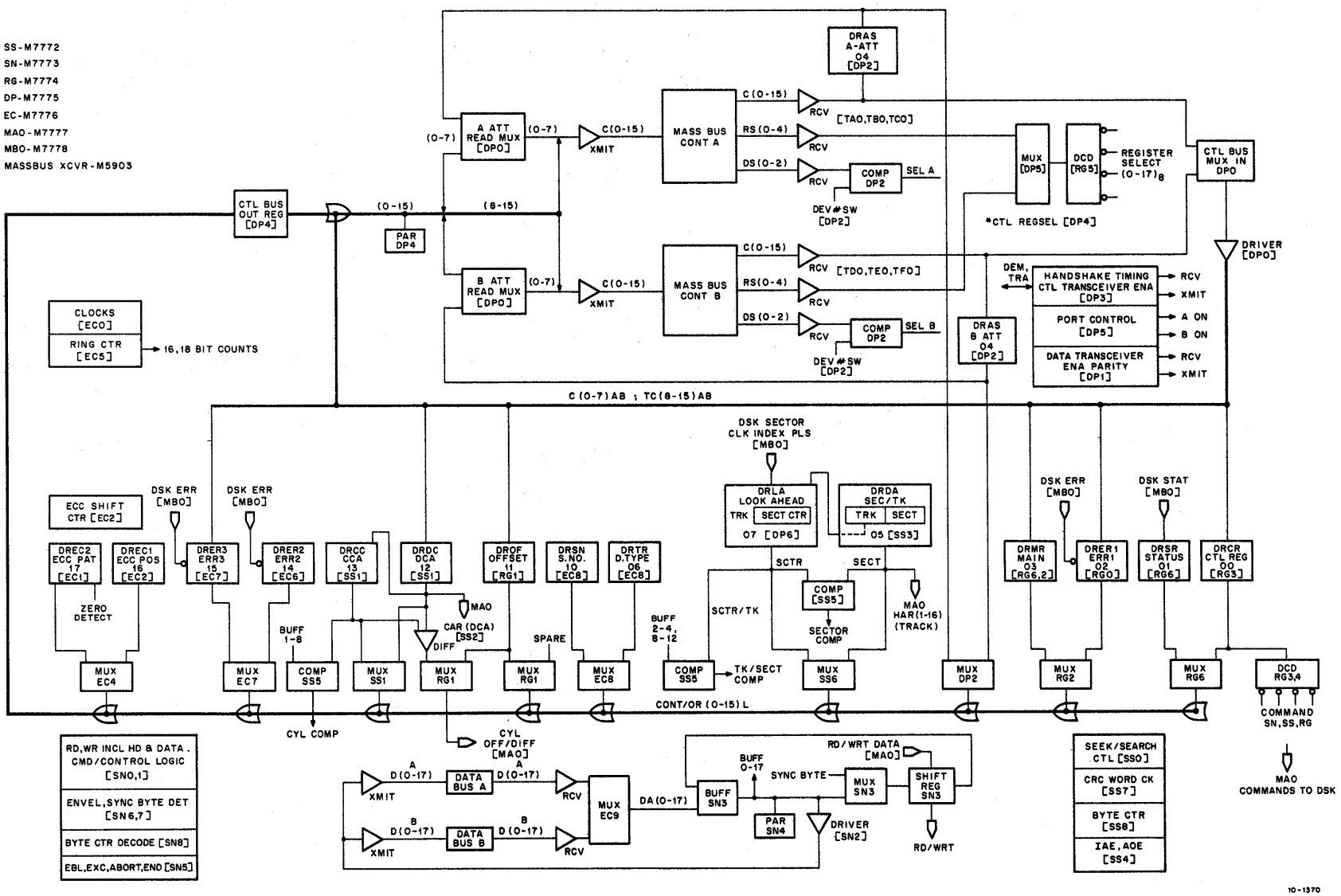


Figure A-2 RP04 DCL Block Diagram

Reader's Comments

RH10 MASSBUS CONTROLLER
MAINTENANCE MANUAL
EK-RH10-MM-002

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